MF 604

MULTIFUNCTION I/O CARD

USER'S MANUAL

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1. Introduction

1.1. General Description

The MF 604 multifunction I/O card is designed for the need of connecting PC compatible computers to real world signals. The MF 604 contains a 100 kHz throughput 12 bit A/D converter with sample/hold circuit, four software selectable input ranges and 8 channel input multiplexer, 4 independent 12 bit D/A converters, 8 bit digital input port and 8 bit digital output port, 4 quadrature encoder inputs with single-ended or differential interface and 5 timers/counters. The card is designed for standard data acquisition and control applications and optimized for use with Real Time Toolbox for MATLAB®. Because of the small size and low power consumption MF 604 can be used not only in desktop computers but also in portable computers and notebooks.

1.2. Features List

The MF 604 offers following features:

- 10 µs 12 bit A/D converter with sample & hold circuit
- 8 channel single ended fault protected input multiplexer
- Software selectable input ranges ±10V, ±5V, 0-10V, 0-5V
- Internal clock & voltage reference
- 4 D/A converters with 12 bit resolution and ±10V output range
- 4 quadrature encoder inputs with single-ended or differential interface
- Software selectable digital input noise filter (0.2 - 50 µs)

- Quadrature input frequency up to 2 MHz
- Software selectable index pulse operation
- 9513A 5 channel timer/counter with 50 ns resolution
- 8 bit TTL compatible digital input port
- 8 bit TTL compatible digital output port
- DIP switch selectable I/O port base address
- Software selectable interrupt
- Requires one 16-bit ISA slot and optional second slot for second connector
- Power consumption 400 mA@+5V, 50 mA@+12V, 50 mA@-12V
- Operating temperature 0°C to +70°C

1.3. Specifications

1.3.1. A/D Converter

Resolution:	12 bits
Number of channels:	8 single ended
Conversion time:	10 µs
Input ranges:	±10V, ±5V, 0-10V, 0-5V, software selectable
Input protection:	±16.5V
Input impedance:	> 10 kΩ

1.3.2. D/A Converter

Resolution:	12 bit
Number of channels:	4
Settling time:	max. 10 µs (1/2 LSB)
Slew Rate:	10 V/µs

Output current:	min. ±5 mA
Short circuit current:	±30 mA
DC output impedance:	0.1 Ω
Load capacitance:	max. 500 pF
Differential nonlinearity:	±1 LSB
Gain drift:	typ. ±5 ppm/K
Zero drift:	typ. ±5 ppmFSR/K

1.3.3. Digital Inputs

Number of bits:	8
Input signal levels:	TTL
Logic 0:	0.8 V max.
Logic 1:	2.0 V min.

1.3.4. Digital Outputs

Number of bits:	8
Output signal levels:	TTL
Logic 0:	0.5 V max. @ 24 mA (sink)
Logic 1:	2.0 V min. @ 15 mA (source)

1.3.5. Quadrature Encoder Inputs

Number of axes:	4 independent
Resolution:	24 bits
Counter modes:	binary, BCD
Index input:	programmable
Inputs:	differential with Schmitt triggers
Input noise filter:	digital, programmable (0.2 - 50 µs)

Input frequency:	max. 2 MHZ
Quadrature modes:	X1, X2, X4

1.3.6. Counters/Timers

Counter chip:	CTS9513A
Number of channels:	5, 4 of them available on I/O connector
Resolution:	16 bits, cascadable up to 80 bits
Clock frequency:	20 MHZ
Conter modes:	up, down, binary, BCD
Triggering:	software, external
Clock source:	internal, prescalers, external
Inputs:	TTL, Schmitt triggers
Outputs:	TTL

2. Hardware Installation

2.1. DIP Switch Settings

SW1-1	SW1-2	SW1-3	SW1-4	I/O address
ON	ON	ON	ON	200H
ON	ON	ON	OFF	220H
ON	ON	OFF	ON	240H
ON	ON	OFF	OFF	260H
ON	OFF	ON	ON	280H
ON	OFF	ON	OFF	2A0H
ON	OFF	OFF	ON	2C0H
ON	OFF	OFF	OFF	2E0H
OFF	**ON**	**ON**	**ON**	**300H**
OFF	ON	ON	OFF	320H
OFF	ON	OFF	ON	340H
OFF	ON	OFF	OFF	360H
OFF	OFF	ON	ON	380H
OFF	OFF	ON	OFF	3A0H
OFF	OFF	OFF	ON	3C0H
OFF	OFF	OFF	OFF	3E0H

Table 1. I/O Address setting using SW1 switch

The bank of four switches (SW1) on the MF 604 specifies the base address of I/O ports on the card. MF 604 occupies 32 consequent addresses in PC's I/O address space. Possible settings of DIP switches are listed in table 1. According to this table selecting I/O address 300H means that switch 1 should be switched OFF while all other switches should be ON. Default factory setting of base address is 300H.

2.2. Installation

Once you have properly set all switches you can install the MF 604 card in any free ISA expansion slot of your computer. Follow the steps outlined below:

- Turn off the power to the computer system and unplug the power cord.
- Disconnect all cables connected to the computer system.
- Using a screwdriver (or nut driver), remove the cover-mounting screws. that screws are at the rear side of the PC.
- Remove the computer system's cover.
- Find an empty expansion slot for in your computer for MF 604 card. If the slot still has the metal expansion-slot cover attached, remove the cover with a screwdriver. Save the screw to install the MF 604.
- Hold the MF 604 firmly at the top of the board, and press the gold edge connector into an empty expansion slot.
- Using a screwdriver (or nut driver), screw the retaining bracket tightly against the rear plate of the computer system.
- In case of using also quadrature encoder inputs or timer/counters install also the aditional connector with metal slot cover to neighbouring slot. Otherwise you can disconnect the aditional connector from the board and save it for future use.
- Replace the cover of the computer, and plug in the power cord.
- Reconnect all cables that were previously attached to the rear of the computer.

3. Programming Guide

3.1. I/O Port Map

I/O space of MF 604 card consists of 32 registers immediately following the base address selected by SW1:

Address	Read	Write
Base+0	**9513A** - Data read	**9513A** - Data write
Base+1	**9513A** - Command read	**9513A** - Command write
Base+2		
Base+3		
Base+4	**DIN** - Digital input register	**DOUT** - Digital output register
Base+5		**IRQEN** - Int. control register
Base+6	**ADLO** - A/D data low byte	**ADCTRL** - A/D control reg.
Base+7	**ADHI** - A/D data high byte	
Base+8	**ADSTAT** - A/D status reg.	**DA0LO** - D/A 0 data low byte
Base+9		**DA0HI** - D/A 0 data high byte
Base+A		**DA1LO** - D/A 1 data low byte
Base+B		**DA1HI** - D/A 1 data high byte

Base+C		**DA2LO** - D/A 2 data low byte
Base+D		**DA2HI** - D/A 2 data high byte
Base+E		**DA3LO** - D/A 3 data low byte
Base+F		**DA3HI** - D/A 3 data high byte
Base+10	**IRC0** - Data read	**IRC0** - Data write
Base+11	**IRC0** - Command read	**IRC0** - Command write
Base+12	**IRC1** - Data read	**IRC1** - Data write
Base+13	**IRC1** - Command read	**IRC1** - Command write
Base+14	**IRC2** - Data read	**IRC2** - Data write
Base+15	**IRC2** - Command read	**IRC2** - Command write
Base+16	**IRC3** - Data read	**IRC3** - Data write
Base+17	**IRC3** - Command read	**IRC3** - Command write

Table 2. I/O Port Map

3.2. A/D Converter

All functions of A/D converter are accessible through four registers.
A/D control register **ADCTRL** is used to select input channel, input range and to start conversion. For ADCTRL bit assignment see table 3.

D7 (MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0** (LSB)
0	1	0	RNG	BIP	A2	A1	A0

BIT	NAME	DESCRIPTION
7		Must be always 0
6		Must be always 1
5		Must be always 0
4	RNG	Selects 10V input range (see table 4)
3	BIP	Selects bipolar input range (see table 4)
2, 1, 0	A2, A1, A0	Selects input channel (see table 5)

Table 3. A/D Control Byte Format

0	**0**	**INPUT RANGE (V)**
0	0	0 to 5
1	0	0 to 10
0	1	± 5
1	1	± 10

Table 4. Input Range Selection

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	*							
0	0	1		*						
0	1	0			*					
0	1	1				*				
1	0	0					*			
1	0	1						*		
1	1	0							*	
1	1	1								*

Table 5. Input Channel Selection

Conversion is initiated with a write operation to **ADCTRL** register (located at address BASE+6) which also selects the input multiplexer channel and input range. When the conversion is complete bit 7 in A/D status register **ADSTAT** (BASE+8) is set to zero. Then the data is ready and can be read from **ADLO** and **ADHI** registers (BASE+6, BASE+7). The read operation of **ADLO** and **ADHI** registers sets the conversion complete bit in **ADSTAT** register back to one. Writing a new control byte during conversion cycle will abort current conversion and start a new conversion cycle.

D7 (MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0** (LSB)
CC	0	0	0	0	0	0	0

Table 6. A/D Status Byte Format

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ADLO	D7	D6	D5	D4	D3	D2	D1	D0
ADHI	0 or D11	0 or D11	0 or D11	0 or D11	D11	D10	D9	D8

Table 7. A/D Data Registers Format

The output data format is binary in unipolar mode and twos-complement binary in bipolar mode. When reading **ADLO** the lower eight bits are read. When reading **ADHI** the upper four MSBs are available and the output data bits D4-D7 are either set 0 (in unipolar mode) or set to the value of MSB (in bipolar mode) as described in Table 7.

A/D converter voltage reference can be adjusted by R11.

Sample code for A/D conversion:

```
unsigned short BASE;
int ch;
short ad;
char Gain[8];
.
.
// start conversion on channel ch
  outp(BASE+6, ch | (Gain[ch]<<3) | 0x40);
// wait until conversion completed
  while (ISBIT1(inp(BASE+8),0x80));
// read data
  ad=inpw(BASE+6);
// convert to bipolar range
  ad-= Gain[ch] & 0x1 ? 0 : 0x800;
// convert to double
  return(ad/(double) (1<<11));
```

3.3. D/A Converters

D/A converters are accessed through eight data input latch registers (**DA0LO, DA0HI, DA1LO, DA1HI, DA2LO, DA2HI, DA3LO, DA3HI**). D/A converters do not require any initialization. Analog outputs are updated when the high byte is written to D/A register. Therefore low byte must be written first for correct operation.

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DALO	D7	D6	D5	D4	D3	D2	D1	D0
DAHI	0	0	0	0	D11	D10	D9	D8

Table 8. D/A Data Registers Format

Output voltage ranges of D/A converters are ±10V. After power-on or hardware reset the output voltage is set to 0V.

Digital input	**Output Voltage**
0xFFF	9.9951 V
0x800	0.0000 V
0x7FF	-0.0049 V
0x000	-10.0000 V

Table 9. D/A Outputs

3.4. Digital I/O

MF 604 contains one 8-bit digital input port and one 8-bit digital output port. Digital input port can be accessed directly by read from **DIN** register (BASE+4). Inputs are TTL compatible. Digital output port can be accessed by write to **DOUT** register (BASE+4). Outputs are TTL compatible. After power-on or hardware reset digital outputs are set to 0.

3.5. Quadrature Encoder Inputs

MF 604 contains four quadrature encoder inputs with single-ended or differential interface and index puls inputs. Inputs are differential TTL compatible with Schmitt triggers. Two LS7266R1 chips with 20 MHz clock are used, first for channels IRC0 and IRC1, second for IRC2 and IRC3. For detail low-level documentation please refer to LS7266R1 documentation in Appendix of this User's Manual.

Each IRC channel has one data register and one command register allowing you to access all internal data and control structures. As internal counters are 24 bit wide **Byte Pointers BP** with autoincrement function are used to address 3 bytes sequentially. Each counter can be loaded from **Preset Register PR** and latched to **Output Latch OL**.

The Read and Write operations on an OL or PR always accesses one byte at a time. The byte that is accessed is addressed by BP. BP is autoincremented at the end of every Read or Write cycle on OL or PR,

lower bytes are accessed first. BP can be reset by **Reset and Load Decoder RLD**.

Each counter has a **Filter Clock Prescaler PSC** which is a programmable modulo-N 8-bit counter driven by chip clock (20 MHz). The divider N can be downloaded to PSC from PR low byte register using **Reset and Load Decoder RLD**. Filter clock frequency = $2x10^7/(n+1)$ where n = PSC = 0 to 0xFF.

RLD allows tranfer PR to CNTR, transfer CNTR to OL, reset CNTR, BP and FLAG.

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Command register bit**
							0	No operation
							1	Reset BP
					0	0		No operation
					0	1		Reset CNTR
					1	0		Reset Borrow, Carry, Compare, Sign flag
					1	1		Reset Error flag
			0	0				No operation
			0	1				Transfer PR to CNTR (24 bits)
			1	0				Transfer CNTR to OL (24 bits)
			1	1				Transfer PR0 to PSC
0	0	0						Select RLD

Table 10. Command register bit assignments for RLD access

Conter Mode Register CMR allows programming of counter operational mode.

7	6	5	4	3	2	1	0	**Command register bit**
							0	Binary count
							1	BCD count
					0	0		Normal count
					0	1		Range limit
					1	0		Non-recycle count
					1	1		Modulo-N
			0	0				Non-quadrature
			0	1				Quadrature X1
			1	0				Quadrature X2
			1	1				Quadrature X4
0	0	1						Select CMR

Table 11. Command register bit assignments for CMR access

For detail description of Range Limit, Non-Recycle and Modulo-N modes refer to LS7266R1 documentation.

Input/Output Control Register IOR controls programmable input and output pins. As MF 604 does not use these pins this register can be used to enable/disable A and B inputs only.

7	6	5	4	3	2	1	0	**Command register bit**
							0	Disable A and B inputs
							1	Enable A and B inputs
0	1	0	0	0	0	0		Select CMR

Table 12. Command register bit assignments for IOR access

Index Control Register IDR allows programming of index operation. Index input is connected to RCNTR/ABG pin and bit 2 of IDR must be set to 1 for correct index operation.

7	6	5	4	3	2	1	0	**Command register bit**
							0	Disable index
							1	Enable index
						0		Negative index polarity
						1		Positive index polarity
0	1	1	0	0	1			Select CMR

Table 13. Command register bit assignments for IDR access

Sample code for IRC operation:

```
/* initialize IRC */

for (i=0; i<IRC_INPUTS; i++)
 {
  outp(BASE+0x11+2*i,0x01);    // reset BP

  outp(BASE+0x10+2*i, 0);      // PR0 = 0
```

```
  outp(BASE+0x11+2*i,0x18);    // PR0 -> PSC
  outp(BASE+0x11+2*i,0x01);    // reset BP
  outp(BASE+0x10+2*i,0x00);    // reset PR
  outp(BASE+0x10+2*i,0x00);
  outp(BASE+0x10+2*i,0x00);
  outp(BASE+0x11+2*i,0x08);    // PR -> CNTR
  outp(BASE+0x11+2*i,0x38);    // CMR
  outp(BASE+0x11+2*i,0x41);    // IOR
  outp(BASE+0x11+2*i,0x65);    // IDR
 }

.
.
/* read IRC */
  ad=BASE+0x10+2*ch;
  outp(ad+1,0x11);    // CNTR -> OL, reset BP
  irc=inp(ad);
  irc+=inp(ad)<<8;
  irc+=inp(ad)<<16;
  return(irc);
```

3.6. Timer/Counter

MF 604 contains CTS9513 timer/counter chip with 20 MHz input clock. The first four timers are accessible through external connector X2 while the fifth timer can generate system interrupt (if enabled by **IRQEN** register) or can be used as a clock source for other timers or for similar internal functions. Gate and clock inputs are connected together and sharing the same input pin (TxIN) on I/O connector. Therefore this pin can be used either as a clock source or as a gate source. Inputs and outputs are TTL compatible, Schmitt triggers are at all inputs to improve noise immunity. CTS9513 timer is connected as 8-bit device. Do not

program it to 16-bit mode.

CTS9513 is a powerfull counter/timer chip offering wide range of operation modes allowing:

- up/down, binary/BCD counting
- internal or external clock and gate sources
- binary/BCD prescaling
- one shot/continuous outputs
- software/external triggering
- programmable gate and output polarities
- time of day and alarm functions
- pulse counting
- frequency measurement
- pulse generation including PWM
- programmable clock source

For detail low-level documentation describing all modes of operation please refer to CTS9513 documentation in Appendix of this User's Manual.

Sample code for programming timer 1 as 1 kHz frequency generator:

```
/* master reset disables all counters/timers, loads
   0x0000 to Master Mode register and all Load and
   Hold registers, loads 0x0B00 to all Counter Mode
   registers, does not reset counter values  */

  outp(BASE+1, 0xFF);  // master reset
  outp(BASE+1, 0x5F);  // resets all counters loading
                       // 0x0000 from Load registers
```

```
/* write 0x0B22 to Counter 1 Mode register to select
   binary mode, counting down without gating, output
   toggle on terminal count, repeat mode, using F1
   clock source (20 MHz)  */

  outp(BASE+1, 0x01);  // select Counter 1 Mode reg.
  outp(BASE, 0x22);    // write Counter 1 Mode reg. LO
  outp(BASE, 0x0B);    // write Counter 1 Mode reg. HI

/* write 10000 (0x2710) to Counter 1 Load register
   will cause counter owerflow and output toggle
   every 0.5 ms and produce 1 kHz squre wave on
   timer/counter 1 output after arming the counter */

  outp(BASE+1, 0x09);  // select Counter 1 Load reg.
  outp(BASE, 0x10);    // write Counter 1 Load reg. LO
  outp(BASE, 0x27);    // write Counter 1 Load reg. HI
  outp(BASE+1, 0x61);  // loads and arms counter 1
```

3.7. IRQEN Register

MF 604 is capable of generating system interrupt on interrupt lines 2, 3, 5, 10, 11, 12 and 15. After power on or hardware reset all interrupts are disabled. Interruprs can be enabled or disabled using **IRQEN** (BASE+5) register. Writing 1 to corresponding bit in **IRQEN** enables interrupt from timer 5 output (not from the timer 5 INT output), 0 disables interrupt. For bit assignment of **IRQEN** register see Table 14. Do not set more than one bit of **IRQEN** register to 1 otherwise more than one interrupt will be enabled.

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IRQ	N/A	15	12	11	10	5	3	2

Table 14. IRQEN Register Bit Assignment

4. I/O Signals

4.1. Output Connector Signal Description

The MF 604 multifunction I/O card is equipped with an on-board 37 pin D-type female connector X1 and with an aditional 37 pin D-type female connector X2 on cable extender. For pin assignment refer to Tables 15 and 16. TB 620 Terminal Board can be connected to both connectors.

AD0-AD7	Analog inputs
DA0-DA3	Analog outputs
DIN0-DIN7	TTL compatible digital inputs
DOUT0-DOUT7	TTL compatible digital outputs
IRC0-IRC3	Quadrature encoder A, B and Index inputs
T0IN-T3IN	Timer/counter gate and clock inputs
T0OUT-T3OUT	Timer/counter outputs
+12V	+12V power supply
-12V	-12V power supply
+5V	+5V power supply
AGND	Analog ground
GND	Digital ground

AD0	**1**	**20**	DA0
AD1	**2**	**21**	DA1
AD2	**3**	**22**	AGND
AD3	**4**	**23**	DA2
AD4	**5**	**24**	DA3
AD5	**6**	**25**	AGND
AD6	**7**	**26**	-12V
AD7	**8**	**27**	+12V
AGND	**9**	**28**	+5V
AGND	**10**	**29**	GND
GND	**11**	**30**	DOUT0
DIN0	**12**	**31**	DOUT1
DIN1	**13**	**32**	DOUT2
DIN2	**14**	**33**	DOUT3
DIN3	**15**	**34**	DOUT4
DIN4	**16**	**35**	DOUT5
DIN5	**17**	**36**	DOUT6
DIN6	**18**	**37**	DOUT7
DIN7	**19**		

Table 15. X1 Connector Pin Assignement

IRC1A+	**1**	**20**	IRC0A+
IRC1A-	**2**	**21**	IRC0A-
IRC1B+	**3**	**22**	IRC0B+
IRC1B-	**4**	**23**	IRC0B-
IRC1I+	**5**	**24**	IRC0I+
IRC1I-	**6**	**25**	IRC0I-
IRC2A-	**7**	**26**	
IRC2A-	**8**	**27**	
IRC2B+	**9**	**28**	+5V
IRC2B-	**10**	**29**	GND
IRC2I+	**11**	**30**	T0IN
IRC2I-	**12**	**31**	T0OUT
IRC3A-	**13**	**32**	T1IN
IRC3A-	**14**	**33**	T1OUT
IRC3B+	**15**	**34**	T2IN
IRC3B-	**16**	**35**	T2OUT
IRC3I+	**17**	**36**	T3IN
IRC3I-	**18**	**37**	T3OUT
GND	**19**		

Table 16. X2 Connector Pin Assignement

Contact address:

HUMUSOFT s.r.o.
Novákových 6
180 00 Praha 8
Czech Republic
tel.: + 420 2 66315767
tel./fax: + 420 2 6844174
E-mail: info@humusoft.cz
Homepage: http//www.humusoft.cz

LSI/CSI

LS7266R1

LSI Computer Systems, Inc. 1235 Walt Whitman Road, Melville, NY 11747 (516) 271-0400 FAX (516) 271-0405

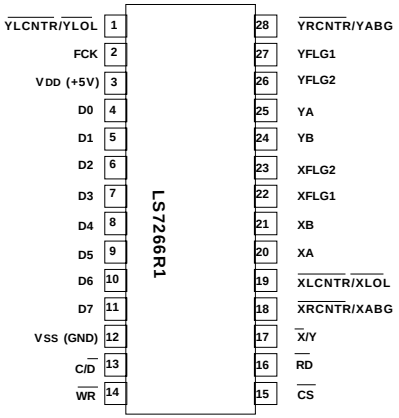
24-BIT DUAL-AXIS QUADRATURE COUNTER

January 1998

FEATURES:

- 30 MHz count frequency in non-quadrature mode, 17MHz in X4 quadrature mode.
- Dual 24-bit counters to support X and Y axes in motion control applications
- Dual 24-bit comparators
- Digital filtering of the input quadrature clocks
- Programmable 8-bit separate filter clock prescalers for each axis
- Error flags for noise exceeding filter band width
- Programmable Index Input and other programmable I/Os.
- Independent mode programmability for each axis
- Programmable count modes: Quadrature (X1, X2, X4) / Non-quadrature, Normal / Modulo-N / Range Limit / Non-Recycle, Binary / BCD.
- 8-bit 3-State data I/O bus
- 5V operation (V_{DD}-V_{SS})
- TTL/CMOS compatible I/Os
- 28-Pin SOIC, 28-Pin PDIP (300mil, 600mil)

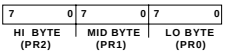
PIN ASSIGNMENT - TOP VIEW
28-Pin Package



LS7266R1 Registers:
LS7266R1 has a set of registers associated with each X and Y axis. All X-axis registers have the name prefix X, whereas all Y-axis registers have the prefix Y. Selection of a specific register for Read/Write is made from the decode of the three most significant bits (D7-D5) of the data-bus. $\overline{CS}$ input enables the IC for Read/Write. C/$\overline{D}$ input selects between control and data information for Read/Write. Following is a complete list of LS7266R1 registers.

Preset Registers: XPR and YPR
Each of these PRs are 24-bit wide. 24-bit data can be written into a PR, one byte at a time, in a sequence of three data write cycles.

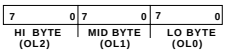
PR



Counters: XCNTR and YCNTR
Each of these CNTRs are 24-bit synchronous Up/Down counters. The count clocks for each CNTR is derived from its associated A/B inputs. Each CNTR can be loaded with the content of its associated PR.

Output Latches: XOL and YOL
Each OL is 24-bits wide. In effect, the OLs are the output ports for the CNTRs. Data from each CNTR can be loaded into its associated OL and then read back on the data-bus, one byte at a time, in a sequence of three data Read cycles.

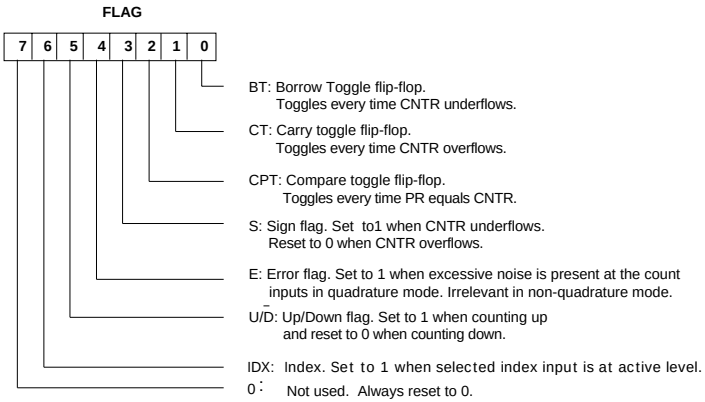
OL



Byte Pointers: XBP and YBP
The Read and Write operations on an OL or a PR always accesses one byte at a time. The byte that is accessed is addressed by one of the BPs. At the end of every data Read or Write cycle on an OL or a PR, the associated BP is automatically incremented to address the next byte.

Flag Register: XFLAG and YFLAG

The FLAG registers hold the status information of the CNTRs and can be read out on the data bus. The E bit of a FLAG register is set to 1 when the noise pulses at the quadrature inputs are wide enough to be validated by the input filter circuits. E = 1 indicates excessive noise at the inputs but not a definite count error. Once set, E can only be reset via the RLD.



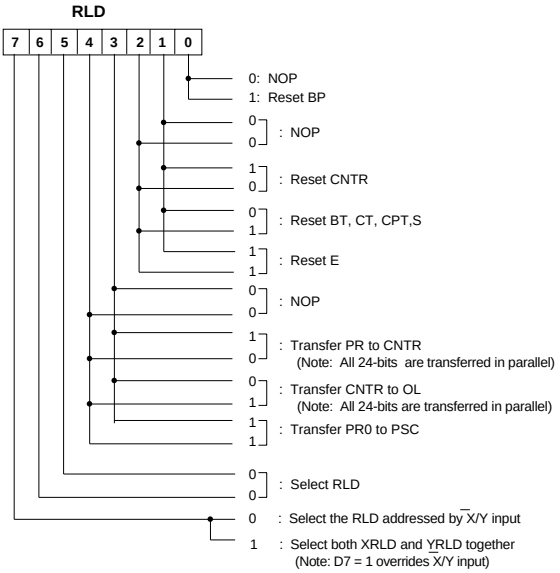
Filter Clock Prescalers: XPSC and YPSC

Each PSC is an 8-bit programmable modulo-N down counter, driven by the FCK clock. The factor N is down loaded into a PSC from the associated PR low byte register PR0. The PSCs provide the ability to generate independent filter clock frequencies for each channel.

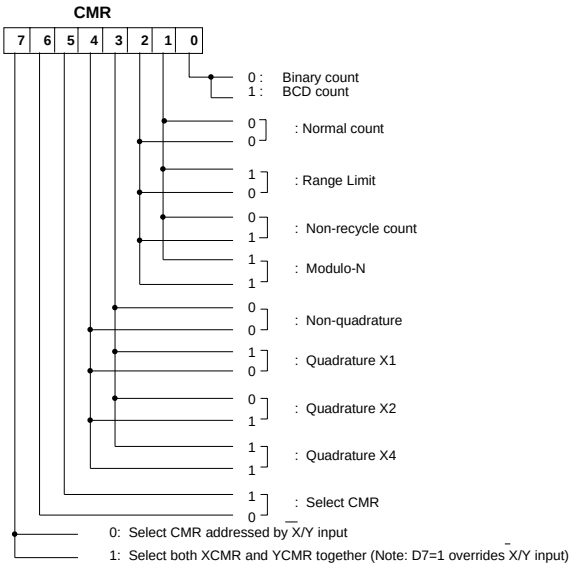
Final filter clock frequency $f_{FCKn} = (f_{FCK}/(n+1))$, where n = PSC = 0 to FF$_H$

Reset and Load Signal Decoders: XRLD and YRLD

Following functions can be performed by writing a control byte into an RLD: Transfer PR to CNTR, Transfer CNTR to OL, reset CNTR, reset FLAG and reset BP.



Counter Mode Registers: XCMR and YCMR
The CNTR operational mode is programmed by writing into the CMRs.



DEFINITIONS OF COUNT MODES:

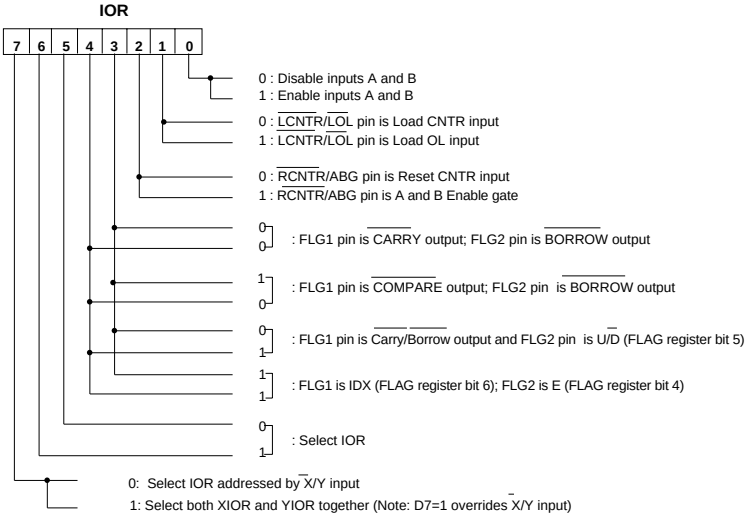
Range Limit. In range limit count mode, an upper and a lower limit is set, mimicking limit switches in the mechanical counterpart. The upper limit is set by the content of the PR and the lower limit is set to be 0. The CNTR freezes at CNTR=PR when counting up and at CNTR=0 when counting down. At either of these limits, the counting is resumed only when the count direction is reversed.

Non-Recycle. In non-recycle count mode, the CNTR is disabled, whenever a count overflow or underflow takes place. The end of cycle is marked by the generation of a Carry (in Up Count) or a Borrow (in Down Count). The CNTR is re-enabled when a reset or load operation is performed on the CNTR.

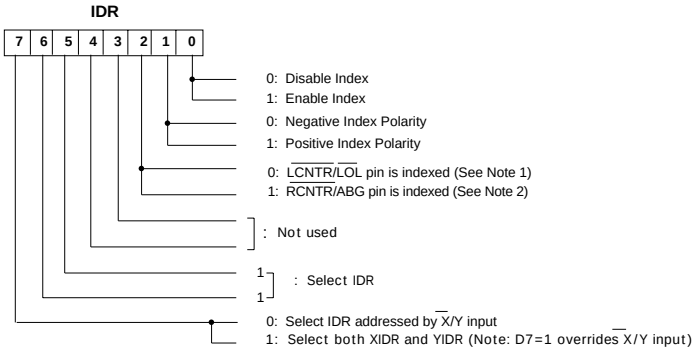
Modulo-N. In modulo-N count mode, a count boundary is set between 0 and the content of PR. When counting up, at CNTR=PR, the CNTR is reset to 0 and the up count is continued from that point. When counting down, at CNTR=0, the CNTR is loaded with the content of PR and down count is continued from that point.

The modulo-N is true bidirectional in that the divide-by-N output frequency is generated in both up and down direction of counting for same N and does not require the complement of N in the UP instance. In frequency divider application, the modulo-N output frequency can be obtained at either the Compare (FLG1) or the Borrow (FLG2) output. Modulo-N output frequency, $f_N = (f_i / (N+ 1))$ where f_i = Input count frequency and N=PR.

Input/Output Control Register: XIOR and YIOR
The functional modes of the programmable input and output pins are written into the IORs.



INDEX CONTROL REGISTERS: XIDR and YIDR
Either the LCNTR/LOL or the RCNTR/ABG inputs can be initialized to operate as an index input. When initialized as such, the index signal from the encoder, applied to one of these inputs performs either the Reset CNTR or the Load CNTR or the Load OL operation synchronously with the quadrature clocks. Note that only one of these inputs can be selected as the Index input at a time and hence only one type of indexing function can be performed in any given set-up. **The index function must be disabled in non-quadrature count mode.**



Note 1 : Function selected for this pin via IOR, becomes the operating INDEX function.

Note 2: RCNTR/ABG input must also be initialized as the reset CNTR input via IOR

REGISTER ADDRESSING MODES

D7	D6	D5	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	X/$\overline{Y}$	$\overline{CS}$	FUNCTION
X	X	X	X	X	X	X	1	Disable both axes for Read/Write
X	X	X	0	1	⌐¬	0	0	Write to XPR byte segment addressed by XBP (Note 3)
X	X	X	0	1	⌐¬	1	0	Write to YPR byte segment addressed by YBP (Note 3)
0	0	0	1	1	⌐¬	0	0	Write to XRLD
0	0	0	1	1	⌐¬	1	0	Write to YRLD
1	0	0	1	1	⌐¬	X	0	Write to both XRLD and YRLD
0	0	1	1	1	⌐¬	0	0	Write to XCMR
0	0	1	1	1	⌐¬	1	0	Write to YCMR
1	0	1	1	1	⌐¬	X	0	Write to both XCMR and YCMR
0	1	0	1	1	⌐¬	0	0	Write to XIOR
0	1	0	1	1	⌐¬	1	0	Write to YIOR
1	1	0	1	1	⌐¬	X	0	Write to both XIOR and YIOR
0	1	1	1	1	⌐¬	0	0	Write to XIDR
0	1	1	1	1	⌐¬	1	0	Write to YIDR
1	1	1	1	1	⌐¬	X	0	Write to both XIDR and YIDR
X	X	X	0	0	1	0	0	Read XOL byte segment addressed by XBP (Note 3)
X	X	X	0	0	1	1	0	Read YOL byte segment addressed by YBP (Note 3)
X	X	X	1	0	1	0	0	Read XFLAG
X	X	X	1	0	1	1	0	Read YFLAG

X = Don't Care

Note 3: Relevant BP is automatically incremented at the trailing edge of $\overline{RD}$ or $\overline{WR}$ pulse

---

Absolute Maximum Ratings:

Parameter	Symbol	Values	Unit
Voltage at any input	V_{IN}	V_{SS}-.3 to V_{DD}+.3	V
Supply Voltage	V_{DD}	+7.0	V
Operating Temperature	T_A	-25 to +80	^oC
Storage Temperature	T_{STG}	-65 to +150	^oC

DC Electrical Characteristics. (T_A = -25°C to +80°C, V_{DD} = 4.5V to 5.5V)

Parameter	Symbol	Min. Value	Max.Value	Unit	Remarks
Supply Voltage	V_{DD}	4.5	5.5	V	-
Supply Current	I_{DD}	-	800	µA	All clocks off
Input Logic Low	V_{IL}	-	0.8	V	-
Input Logic High	V_{IH}	2.0	-	V	-
Output Low Voltage	V_{OL}	-	0.5	V	I_{OSNK}=5mA
Output High Voltage	V_{OH}	V_{DD}-.5	-	V	I_{OSRC}=1mA
Input Leakage Current	I_{ILK}	-	30	nA	-
Data Bus Leakage Current	I_{DLK}	-	60	nA	Data bus off
Output Source Current	I_{OSRC}	1.0	-	mA	V_O = V_{DD}-.5V
Output Sink Current	I_{OSNK}	5.0	-	mA	V_O = 0.5V

Transient Characteristics. (T_A = -25˚C to +80˚C, V_{DD} = 4.5V to 5.5V)

Parameter	Symbol	Min. Value	Max.Value	Unit	Remarks
Read Cycle (See Fig. 1)					
$\overline{RD}$ Pulse Width	t_{r1}	50	-	ns	-
$\overline{CS}$ Set-up Time	t_{r2}	50	-	ns	-
$\overline{CS}$ Hold Time	t_{r3}	0	-	ns	-
C/$\overline{D}$ Set-up Time	t_{r4}	50	-	ns	-
C/$\overline{D}$ Hold Time	t_{r5}	10	-	ns	-
$\overline{X}$/Y Set-up Time	t_{r6}	50	-	ns	-
$\overline{X}$/Y Hold Time	t_{r7}	10	-	ns	-
Data Bus Access Time	t_{r8}	50	-	ns	Access starts when both $\overline{RD}$ and $\overline{CS}$ are low.
Data Bus Release Time	t_{r9}	-	25	ns	Release starts when either $\overline{RD}$ or $\overline{CS}$ is terminated.
Back to Back Read delay	t_{r10}	60	-	ns	-
Write Cycle (See Fig. 2)					
$\overline{WR}$ Pulse Width	t_{w1}	30	-	ns	-
$\overline{CS}$ Set-up Time	t_{w2}	30	-	ns	-
$\overline{CS}$ Hold Time	t_{w3}	0	-	ns	-
C/$\overline{D}$ Set-up Time	t_{w4}	30	-	ns	-
C/$\overline{D}$ Hold Time	t_{w5}	10	-	ns	-
$\overline{X}$/Y Set-up Time	t_{w6}	30	-	ns	-
$\overline{X}$/Y Hold Time	t_{w7}	10	-	ns	-
Data Bus Set-up Time	t_{w8}	30	-	ns	-
Data Bus Hold Time	t_{w9}	10	-	ns	-
Back to Back Write Delay	t_{w10}	60	-	ns	-
Quadrature Mode (See Fig. 3-5)					
FCK High Pulse Width	t_1	14	-	ns	-
FCK Low Pulse Width	t_2	14	-	ns	-
FCK Frequency	f_{FCK}	-	35	MHz	-
Mod-n Filter Clock(FCKn)Period	t_3	28	-	ns	t_3 = (n+1) (t_1+t_2), where n = PSC= 0 to FF_H
FCKn frequency	f_{FCKn}	-	35	MHz	-
Quadrature Separation	t_4	57	-	ns	$t_4 \geq 2t_3$
Quadrature Clock Pulse Width	t_5	115	-	ns	$t_5 \geq 4t_3$
Quadrature Clock frequency	f_{QA}, f_{QB}	-	4.3	MHz	$f_{QA} = f_{QB} = 1/8t_3$
Quadrature Clock to Count Delay	t_{Q1}	$5t_3$	$6t_3$	-	-
X1/X2/X4 Count Clock Pulse Width	t_{Q2}	28	-	ns	$t_{Q2} = t_3$
Index Input Pulse Width	t_{idx}	85	-	ns	$t_{idx} \geq 3t_3$
Index Skew from A	t_{Ai}	-	28	ns	$t_{Ai} \leq t_3$
Carry/Borrow/Compare Output Width	t_{Q3}	28	-	ns	$t_{Q3} = t_3$
Non-Quadrature Mode (See Fig. 6-7)					
Clock A - High Pulse Width	t_6	16	-	ns	-
Clock A - Low Pulse Width	t_7	16	-	ns	-
Direction Input B Set-up Time	t_{8S}	20	-	ns	-
Direction Input B Hold Time	t_{8H}	20	-	ns	-
Gate Input (ABG) Set-up Time	t_{GS}	20	-	ns	-
Gate Input (ABG) Hold Time	t_{GH}	20	-	ns	-
Clock Frequency (non-Mod-N)	f_A	-	30	MHz	f_A = (1/ (t_6 + t_7))
Clock Frequency (Mod-N)	f_{AN}	-	25	MHz	-
Clock to Carry or Borrow Out Delay	t_9	-	30	ns	-
Carry or Borrow Out Pulse Width	t_{10}	16	-	ns	$t_{10} = t_7$
Load CNTR, Reset CNTR and Load OL Pulse Width	t_{11}	20	-	ns	-
Clock to Compare Out Delay	t_{12}	50	-	ns	-

INPUTS/OUTPUTS

X-AXIS I/Os:

XA (Pin 20) X-axis count input A
XB (Pin 21) X-axis count input B

Either quadrature encoded clocks or non-quadrature clocks can be applied to XA and XB. In quadrature mode XA and XB are digitally filtered and decoded for UP/DN clock. In non-quadrature mode, the filter and the decoder circuits are by-passed. Also, in non-quadrature mode XA serves as the count input and XB as the UP/DOWN direction control input, with XB = 1 selecting Up Count mode and X_B = 0, selecting Down Count mode.

$\overline{\text{XLCNTR}}$/$\overline{\text{XLOL}}$ (Pin 19) X-axis programmable input, to operate as either direct load XCNTR or direct load XOL or synchronous load XCNTR or synchronous load XOL. The synchronous load mode is intended for interfacing with the encoder Index output in quadrature clock mode. In direct load mode, a logic low level is the active level at this input. In synchronous load mode the active level can be programmed to be either logic low or logic high. Both quarter-cycle and half-cycle Index signals are supported by this input in the indexed Load mode. The synchronous function must be disabled in non-quadrature count mode (See description of IDR on P. 4)

$\overline{\text{XRCNTR}}$/XABG (Pin 18) X-axis programmable input to operate either as direct reset XCNTR or count enable/disable gate or synchronous reset XCNTR. The synchronous reset XCNTR mode is intended for interfacing with the encoder Index output in quadrature clock mode. In direct reset XCNTR mode, a logic low level is the active level at this input whereas in synchronous reset XCNTR mode the active level can be programmed to be either a logic low or a logic high. Both quarter-cycle and half-cycle index signals are supported by this input in the indexed reset CNTR mode. The synchronous function must be disabled in non-quadrature count mode (See description of IDR on P. 4). In count enable/disable mode, a logic high at this input enables the counter and a logic low level disables the counter.

XFLG1 (Pin 22) X-axis programmable output to operate either as XCARRY (Active low), or XCOMPARE (generated when XPR=XCNTR; Active low), or XIDX (XFLAG bit 6) or XCARRY/XBORROW (Active low).

XFLG2 (Pin 23) X-axis programmable output to operate as either XBORROW (Active low) or XU/$\overline{\text{D}}$ (XFLAG bit 5) or XE (XFLAG bit 4).

Y-AXIS I/Os:

All the X-axis inputs/outputs are duplicated for the Y-axis with similar functionalities.

YA (Pin 25)
YB (Pin 24)
$\overline{\text{YLCNTR}}$/YLOL (Pin 1)
YRCNTR/YABG (Pin 28)
YFLG1 (Pin 27)
YFLG2 (Pin 26)

COMMON I/Os:

$\overline{\text{WR}}$ (Pin 14) Write input. Control/data bytes are written at the trailing edge of low level pulse applied to this input.

$\overline{\text{RD}}$ (Pin 16) Read input. A low level applied to this input enables the FLAGs and OLs to be read on the data bus.

$\overline{\text{CS}}$ (Pin 15) Chip select input. A low level applied to this input enables the chip for Read and Write.

C/$\overline{\text{D}}$ (Pin 13) Control/Data input. This input selects between a control register or a data register for Read/Write. When low, a data register is selected. When high, a control register is selected.

D0-D7 (Pins 4-11) Data Bus input/output. The 8-bit three-state data bus is the I/O port through which all data transfers take place between the LS7266R1 and the host processor.

FCK (Pin 2) Filter clock input in quadrature mode. The FCK is divided down internally by two 8-bit programmable prescalers, one for each channel.

$\overline{\text{X}}$/Y (Pin 17) Selects between X and Y axes for Read or Write. $\overline{\text{X}}$/Y = 0 selects X-axis and $\overline{\text{X}}$/Y = 1 selects Y-axis. $\overline{\text{X}}$/Y is overridden by D7 =1 in Control Write Mode (C/$\overline{\text{D}}$ = 1).

V_{DD} (Pin 3) +5VDC

V_{SS} (Pin 12) GND

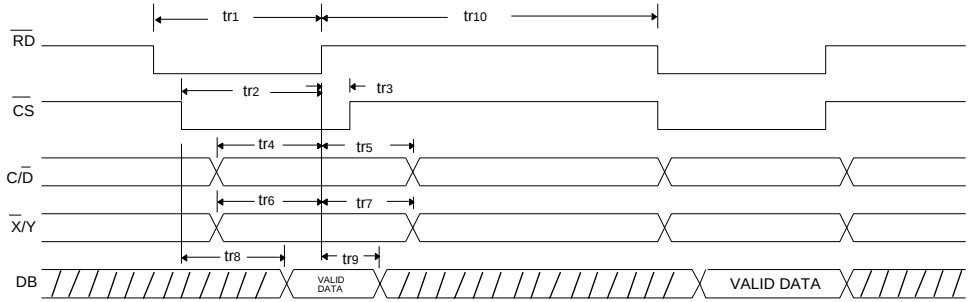


FIGURE 1. READ CYCLE

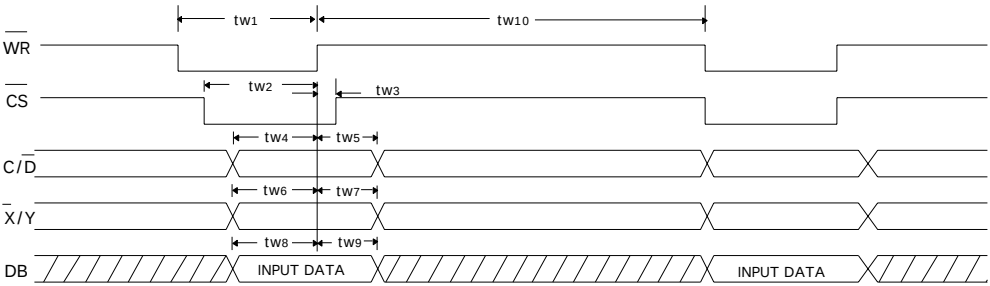


FIGURE 2. WRITE CYCLE

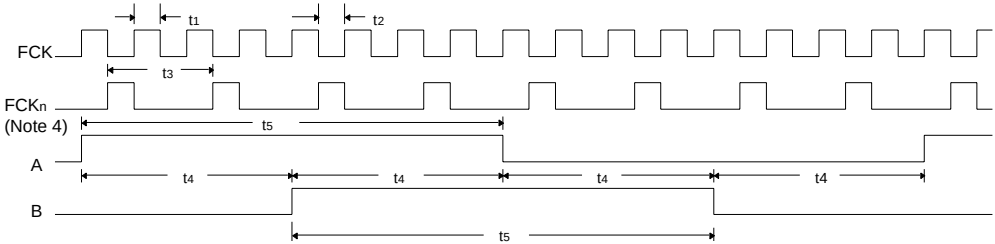


FIGURE 3. FILTER CLOCK FCK AND QUADRATURE CLOCKS A AND B

Note 4: FCKn is the final modulo-n internal filter clock, arbitrarily shown here as modulo-1.

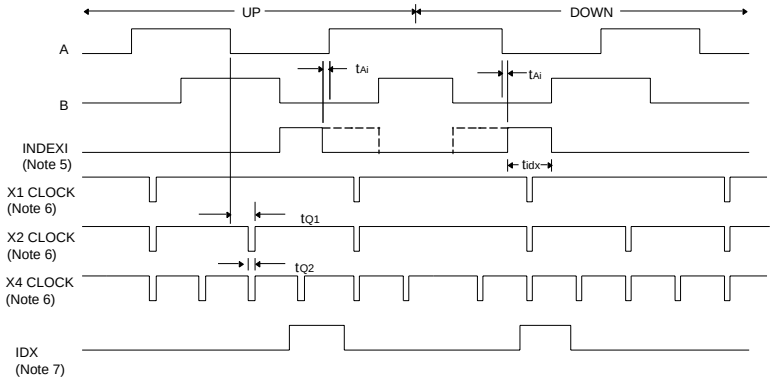


FIGURE 4. QUADRATURE CLOCK A, B AND INDEX INPUT

Note 5: Shown here is positive index with solid line depicting 1/4 cycle index and dotted line depicting 1/2 cycle index. Either LCNTR/LOL or RCNTR/ABG input can be used as the INDEX input.

Note 6: X1, X2 and X4 clocks are the final internal Up/Down count clocks derived from filtered and decoded Quadrature Clock inputs, A and B.

Note 7: IDX is the synchronized internal "load OL" or "load CNTR" or "reset CNTR" signal based on $\overline{\text{LCNTR}}/\overline{\text{LOL}}$ or RCNTR/ABG input being selected as the INDEX input, respectively. This signal is identical with FLAG register bit 6.

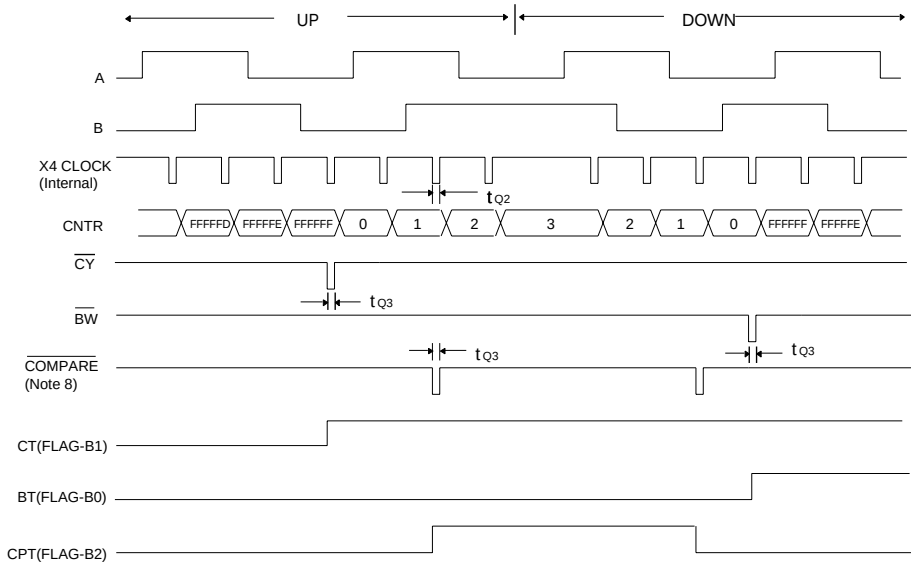


FIGURE 5. CARRY, BORROW, COMPARE, CARRY TOGGLE, BORROW TOGGLE AND COMPARE TOGGLE IN X4 QUADRATURE, NORMAL, BINARY COUNT MODE.

Note 8: $\overline{\text{COMPARE}}$ is generated when PR = CNTR. In this timing diagram it is arbitrarily assumed that PR = 1.

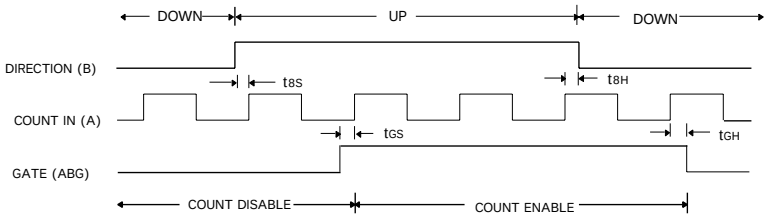


FIGURE 6. COUNT (A), DIRECTION (B) AND GATE (ABG) INPUTS IN NON-QUADRATURE MODE

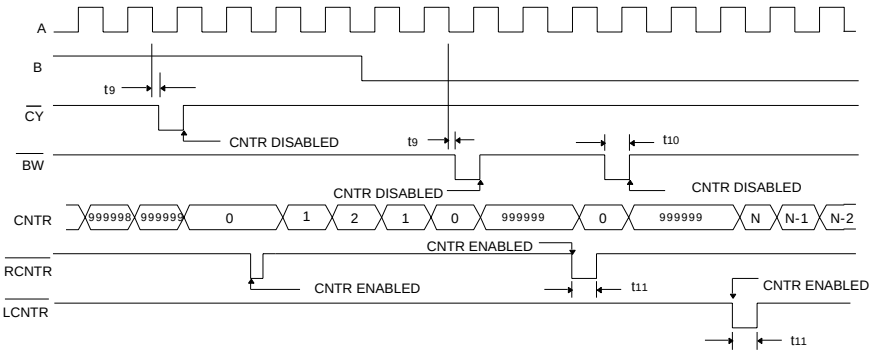


FIGURE 7. NON-RECYCLE, NON-QUADRATURE, BCD MODE

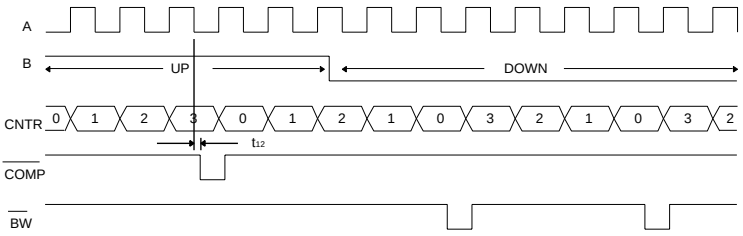


FIGURE 8. MODULO - N, NON-QUADRATURE (Shown with N = 3)

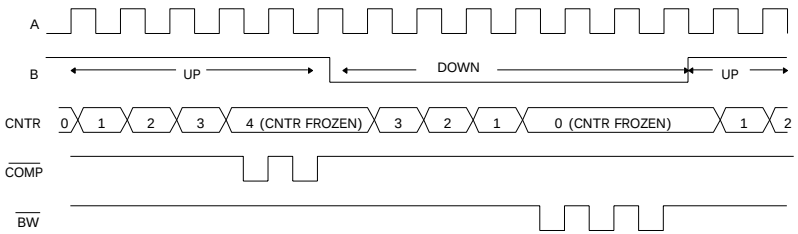
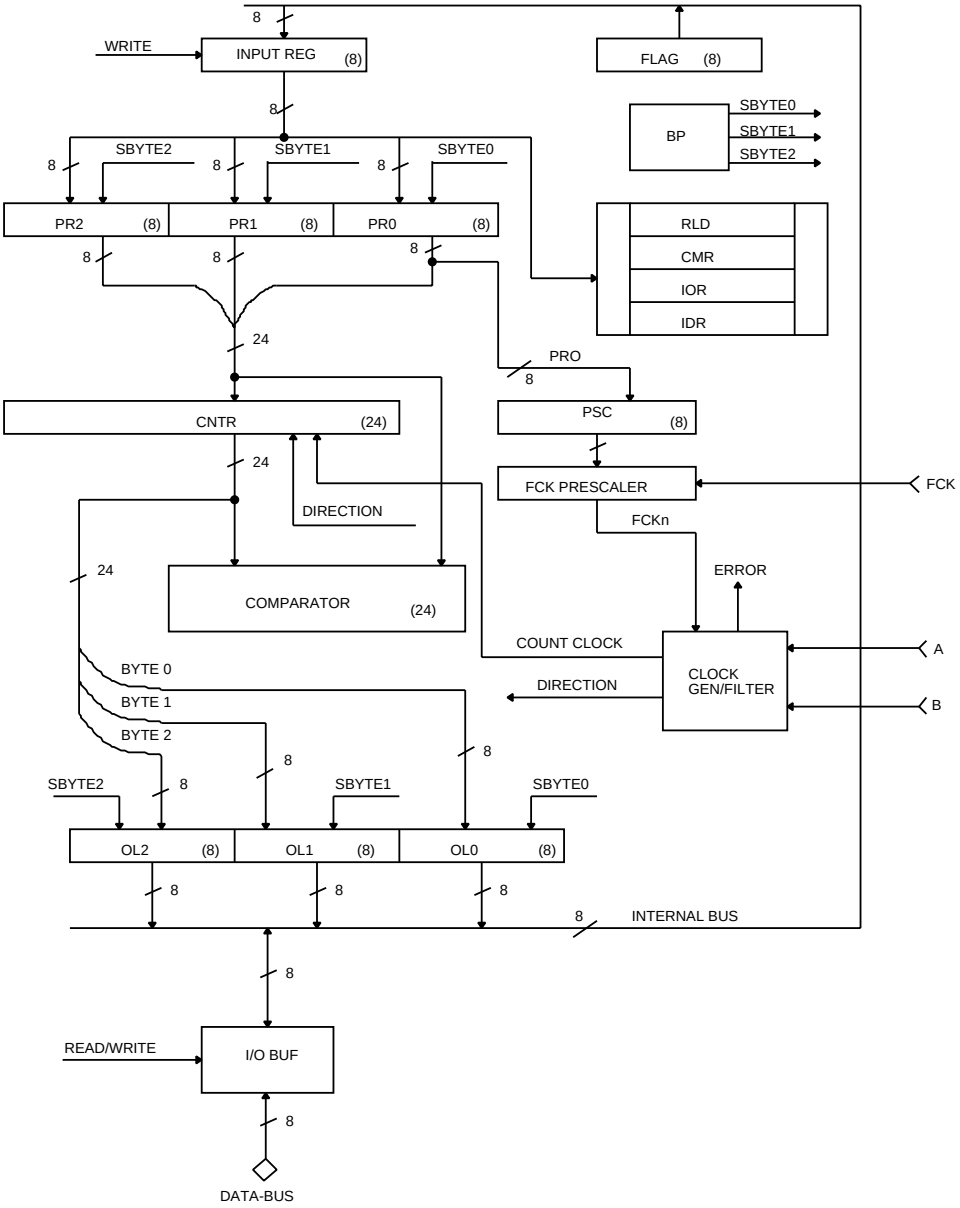


FIGURE 9. RANGE LIMIT, NON-QUADRATURE (Shown with PR = 4)


8
WRITE
INPUT REG (8)
FLAG (8)
8
BP
SBYTE0
SBYTE1
SBYTE2
8
SBYTE2
8
SBYTE1
8
SBYTE0
PR2 (8)
PR1 (8)
PR0 (8)
RLD
CMR
IOR
IDR
8
8
8
24
PRO
8
CNTR (24)
PSC (8)
24
FCK PRESCALER
FCK
DIRECTION
FCKn
24
COMPARATOR (24)
ERROR
COUNT CLOCK
A
BYTE 0
DIRECTION
CLOCK GEN/FILTER
BYTE 1
B
BYTE 2
8
8
SBYTE2
8
SBYTE1
SBYTE0
OL2 (8)
OL1 (8)
OL0 (8)
8
8
8
8
INTERNAL BUS
8
READ/WRITE
I/O BUF
8
DATA-BUS

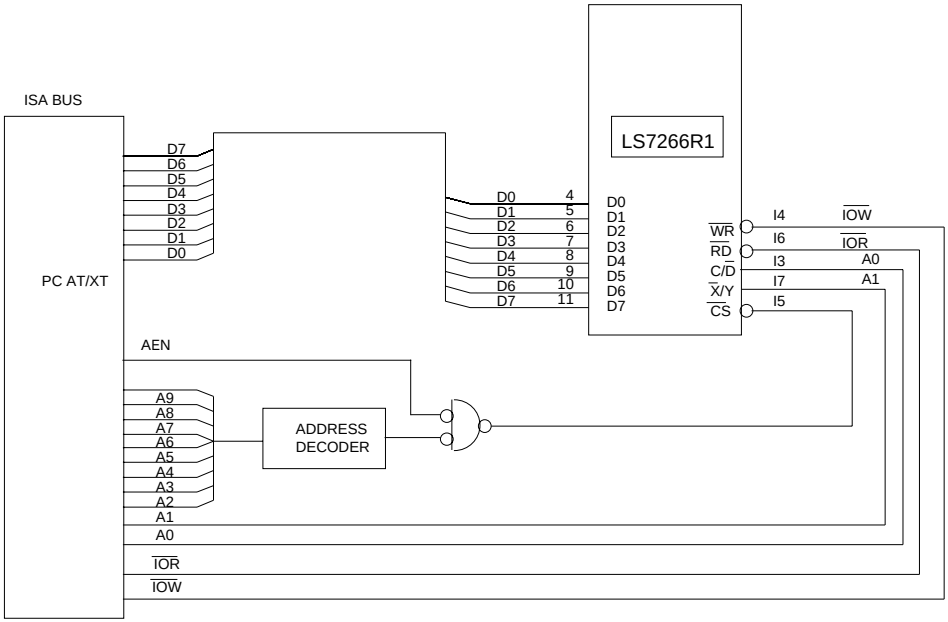


FIGURE 11A. LS7266R1 INTERFACE EXAMPLES

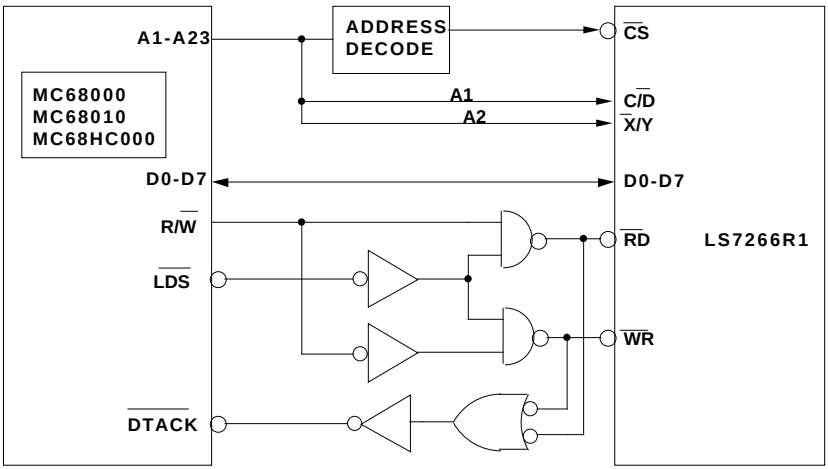


FIGURE 11B. LS7266R1 INTERFACE EXAMPLES

Celeritous Technical Services Corp *806.783.0904*
PO Box 65600-1200 *FAX 806.783.0905*
Lubbock, Texas 79464-5600 *http://www.celeritous.com*

CTS9513
5 Chan 16 bit 50MHz Counter/Timer

FUNCTIONS

- Five 16 bit programmable up/down counters
- Programmable Pulse Generation
- Programmable Delay Generator
- Pulse Measurement
- Event Counting
- Frequency Measurement
- System Synchronization
- Real Time Clock

APPLICATIONS

- Computer System Timing
  - Real Time Clock with Alarm
  - Watchdog Timer
  - Programmable System/Bus Clock
  - Wait State Generation
- Data Acquisition
  - Programmable Converter Clock
  - Pulse Measurement
  - Frequency Counter
  - Event Counter
- ATE
  - Programmable Stimulus Generator
  - Timing Extremes Generator
- Laser Systems
  - Timing Sequencer
  - Programmable Delay Generator
  - External Equipment Synchronization
  - Burst Mode Generator
- Industrial Process Control
  - Pulse Frequency Sensor conversion
  - System Timing/Synchronization

EXTENDED AM9513 FEATURES *(-5 DEVICE)*

- Up to 50 MHz Maximum input frequency
- Extended Pre-scaling
- Internal Interrupt Generation
- Master Output Inhibit
- Extended Count Source Selection

STANDARD AM9513 FEATURES

- Five independent 16 bit counters
- Up/Down, Binary/BCD Counting
- Internal Binary/BCD Prescaling
- One Shot/Continuous Outputs
- Software/External triggering
- Tri-state Outputs
- Programmable output polarities
- Programmable gate polarities/edges
- Time of Day/Alarm Functions
- Programmable Internal/External Counter Source
- Fully AM9513 Hardware/Software Compatible
- Dual count registers on each counter

Figure 1 - CTS9513 DIP-40 Package

CTS9513 OVERVIEW

For two decades the most flexible counter/timer peripheral device available was the Advanced Micro Devices AM9513 Counter Timer. Until discontinued in 1995 the AM9513 was a leading device in industrial and scientific timing controllers. Its only limitation was its 7 Mhz maximum clock speed… … …. *.until now*.....

Building on two decades of successful use as the most flexible programmable counter/timer device, the CTS9513 breaks the old limitations of the AM9513 in a new technology device with over 5 times the performance of the venerable 9513 with 16 bit counters. Sporting up to a 50 MHz Maximum Input clock, the CTS9513 allows timing resolutions of 20 ns and gate pulses as short as 10nS. This opens up a whole new range of capabilities and applications for this device.

The CTS9513 is fully Hardware and Software compatible with the AM9513, allowing use of your present software drivers. The CTS9513-5 Also features an extended set of instructions for additional prescaling of the input clock and internal interrupt generation circuitry Standard Packaging for the CTS9513 is the DIP-40, PLCC-44 PQFP-100 Package. Extended I/O is available in the PQFP-100 package only. Both Commercial and Industrial temperature ranges are available in plastic packaging.

CTS95130

Also in the works is a full 5 x 32 bit implementation of the 9513 capable of 33 Mhz clock speeds. Imagine counter dynamic ranges of 30 nS to over 2 minutes in a single counter. The 33 Mhz clock speed and full 32 bit data path make this a perfect PCI bus compatible peripheral device.

DEVICE DESCRIPTION

The CTS9513 is a custom, high speed gate array implementation and extension of the AMD AM9513 System Timing Controller. The 9513 has long been the most versatile counter/timer peripheral device, featuring far more flexibility than competing timing devices such as the Intel 8253/8254, Motorola 6840 or others. A large installed base of devices and software drivers already exists.

The principal limitation of the AM9513 was its maximum frequency limitation of 7 Mhz imposed by its late 1970's NMOS LSI design. The CTS9513 shatters this barrier with a 50 MHz maximum clock speed.

The CTS9513 Counter/Timer is capable of a wide variety of applications including, but not limited to:

- Event Counting
- Event Sequencing
- Programmable pulse generation
- Programmable delay generation
- Frequency counting
- Frequency synthesis
- Real Time Clock
- Alarm Clock Functions
- Watchdog Timing
- Retriggerable Pulse Generation
- Non-Retriggerable Pulse Generation
- Frequency Shift Keying
- Baud Rate Clock
- Waveform Analysis
- Interrupt Generation
- Pulse burst generation

The user has total software control over key features such as:

- Output Polarities
- Output Impedance
- Input Trigger, Edge Polarities
- Hardware gating/triggering
- Software gating/triggering
- Count Up/Down
- BCD/Binary Counting
- Real time count register read
- Internal counter concatenation (up to 80 bits)
- Programmable frequency source selection
- Programmable internal clock pre-scaling

EXTENDED FEATURES

BACKWARDS COMPATIBLE

The CTS9513 maintains full backwards compatibility with the AM9513. allowing continued use of your existing software drivers. Data may be transferred in 8 or 16 bit increments. All internal data paths in the CTS9513 are 16 bit. All 9513 commands registers and modes are supported. Timer commands are still 8 bit, with extended features making use of previously unused commands.

DEVIATIONS FROM THE 9513

The primary hardware feature NOT implemented in the CTS9513 is the GATE1A-GATE5A input lines, shared with the upper 8 bit data bus lines due to their limited utility.

EXTENDED I/O

Interrupt Outputs (PQFP-100 Pkg only)
Five separate interrupt output lines are provided in the CTS9513(PQFP-100 package only), driven by the terminal count pulse of each counter. These lines may be programmed to assert a pulse or a latched level reset by software for use in a variety of processor and bus systems.

Timer Output Inhibit (PQFP-100 Pkg only)
In addition to the software programmable output inhibit or tri-state command, the CTS9513 (PQFP-100 package only) provides a hardware output inhibit signal which overrides all software commands to place the outputs in a high impedance state. This allows external hardware interlock control over the counter outputs. An extension to the Status register allows software monitoring of the state of this line.

FEATURE EXTENSIONS

Auxiliary Master Mode Register
An auxiliary Master Mode Register has been added to accommodate programming of new features. The primary Master Mode Register remain the same as in the 9513 for software compatibility. At power-on and at reset both Master Mode registers are reset to all zeros. If no subsequent writes are made to the auxiliary Master Mode register or as long as all writes are zero filled in the high word, there is no difference in operation from the 9513 as extended features will not be enabled.

Symbol	Description	Min	Max	Units
V_{DD}	DC Supply Voltage	-0.3	7	Volts
V_{IN}	Input Voltage at Any Pin	-0.3	$V_{DD+.3}$	Volts
T_{OP}	Operating Temperature AxC (AxI)	0 (-40)	70 (85)	°C
T_{ST}	Storage Temperature	-55	150	°C

Table 1. Absolute Maximum Ratings

Auxiliary Counter Mode Register
The Auxiliary Counter Mode Register has been added to accommodate extended feature programming. The primary Counter Mode Register remains the same as in the 9513 for software compatibility. At power-on and at reset both Counter Mode registers are reset to all zeros. If no subsequent writes are made to the auxiliary Counter Mode register there is no difference in operation from the 9513 as extended features will not be enabled.

Status Register
The Status register has been extended to 16 bits to accommodate monitoring of the status of the comparators, interrupt outputs and the hardware output inhibit line. The lower 8 bits remain the same as in the 9513 to preserve software compatibility.

24 bit Extended Internal Prescaling
The original 9513 was limited to a maximum of 16 bits of prescaling (,10,000 BCD, ,65,536 Binary). With a 50 MHz clock this would provide limited prescaling to 5kHz in BCD mode or 763 Hz in Binary mode. The CTS9513 extends the internal prescaling counter to 24 bits (, 1M BCD, ,16.77M Binary), adding two additional prescaler outputs. These two new outputs may be programmed as count sources for any of the five counters as well as the FOUT dividers.

FOUT Prescaler
The FOUT counter has been extended to 6 bits. The FOUT counter may now be programmed for divide by 1 to 63 inclusive. The original four bit Master Mode register counter program controls the least significant four bits of FOUT to provide maximum backwards compatibility. The auxiliary Master Mode register contains the program bits for the additional divider.

Command Registers
The command register remains the same as the 9513, with only the lower 8 bits used. Previously unused commands in the 9513 are utilized for the extended features such as Interrupt output control and auxiliary register addressing. This preserves the original two port address access for the timer.

INTERFACE SIGNALS

PACKAGING

Figure 2 illustrates the DIP-40 Package pinout of the device which conforms to the original AM9513 pinouts.

Table 2 summarizes the pinouts of the PLCC-44 package illustrated in Figure 3 which conform to the original AM9513 pinouts.

Table 3 summarizes the CTS9513 device pinouts and signal names for the QFP-100 package illustrated in Figure 4. Pinouts are optimized for ease of layout.

CTSC9513A	x	x	-	x
Package				
Plastic DIP-40	P			
Plastic PLCC-44	J			
Plastic PQFP-100	Q			
Temperature Range				
Commercial (0-70º C)		C		
Industrial (-40 - 85º C)		I		
Maximum Clock Speed				
20 MHz				2
50 MHz				5

Table 2 - CTS9513 Ordering Information

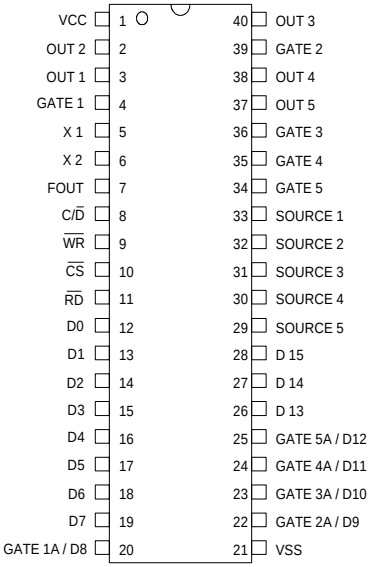


Figure 2 - CTS9513 DIP-40 Package Pinouts

PLCC-44 Package Pinouts			
Pin	**Signal**	**Pin**	**Signal**
1	VCC	23	D8
2	OUT2	24	VSS
3	NC	25	D9
4	OUT1	26	D10
5	GATE1	27	D11
6	X1	28	D12
7	X2	29	D13
8	FOUT	30	D14
9	NC	31	D15
10	C/D	32	NC
11	WR	33	SOURCE5
12	CS	34	SOURCE4
13	RD	35	SOURCE3
14	NC	36	SOURCE2
15	D0	37	SOURCE1
16	D1	38	GATE5
17	D2	39	GATE4
18	D3	40	GATE3
19	D4	41	OUT5
20	D5	42	OUT4
21	D6	43	GATE2
22	D7	44	OUT3

Table 2. PLCC-44 Pinouts

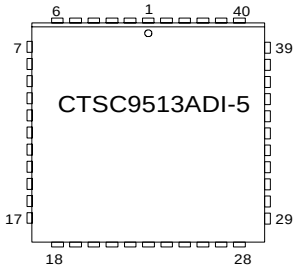


Figure 3. PLCC-44 Outline

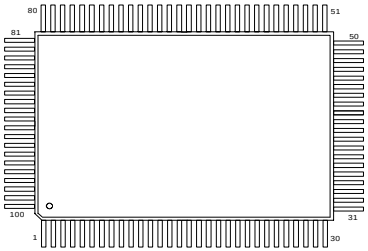


Figure 4. PQFP Package Outline

* Extended Function Pins			
Pin	Signal	Pin	Signal
1	Vcc	51	Vcc
2	D0	52	NC
3	D2	53	NC
4	D4	54	NC
5	D6	55	NC
6	D8	56	NC
7	D10	57	NC
8	D12	58	NC
9	D14	59	NC
10	NC	60	NC
11	NC	61	!RD
12	NC	62	!CS
13	NC	63	NC
14	NC	64	NC
15	NC	65	NC
16	NC	66	NC
17	NC	67	NC
18	C/D	68	NC
19	NC	69	NC
20	!WR	70	NC
21	NC	71	NC
22	NC	72	D15
23	NC	73	D13
24	NC	74	D11
25	NC	75	D9
26	NC	76	D7
27	NC	77	D5
28	NC	78	D3
29	NC	79	D1
30	Vss	80	Vss
31	Vss	81	Vss
32	NC	82	NC
33	NC	83	X1
34	NC	84	NC
35	NC	85	X2
36	NC	86	NC
37	NC	87	SOURCE 1
38	INT 5*	88	SOURCE 2
39	INT 4*	89	SOURCE 3
40	INT 3*	90	SOURCE 4
41	INT 2*	91	SOURCE 5
42	INT 1*	92	NC
43	OUT 5	93	GATE 1
44	OUT 4	94	GATE 2
45	OUT 3	95	GATE 3
46	OUT 2	96	GATE 4
47	OUT 1	97	GATE 5
48	NC	98	NC
49	FOUT	99	!OUTEN*
50	Vcc	100	Vcc

Table 3. PQFP-100 Package Pinouts - * New Signal

ORIGINAL SIGNALS

The following signal names and description conform to the original AM9513 device.

VCC
+5 Volt Power Supply

VSS
Ground

X1
External Crystal. Crystal should be parallel resonant, fundamental mode type. When driven from an external source, X1 should be left open

X2
External Crystal. If driven from an external source X2 should be connected to a TTL source and pulled up to VCC

FOUT (Frequency Divider Outputs)
The FOUT line is generated by internally programmable counters. The clock source for these counters may be any of the external GATE or SOURCE inputs as well as any of the internally prescaled clock outputs.

SOURCE1-5 (Count Source Inputs)
Source inputs 1-5 provide external clock source lines which may be routed to any of the internal counters or the FOUT divider. The active count edge for the source is programmed at the counter.

GATE1-5 (Counter Gate Inputs)
Gate inputs are used to control counter behavior. Any gate may be routed to one of three internal counters. They may also be used as clock or count input sources for the internal counters or FOUT divider. The GATE lines may be programmed for use as counter enables, counter triggers or inhibits and to switch between two different frequencies. Individual counters may be programmed for active polarity as well as to be level or edge sensitive to the GATE line.

In the CTS9513 the auxiliary GATEN/A lines which were originally multiplexed with Data lines D8-12 in the AM9513 are not implemented.

OUT1-5 (Counter Outputs)
OUT1-5 are associated with individual counters. Outputs are tri-state and may be programmed by the counter for output polarity, initialized to a given state and programmed for pulse, square wave or complex duty cycle waveforms. Counter outputs may also be driven into tri-state by the OUTEN line (available in PQFP Package only).

D0-15 (Data Bus)
D0-15 form a bi-directional 16 bit data bus for exchanging programming and status information with a host processor, or system. These lines act as inputs to the counter when CS and WR are asserted and as outputs when RD and CS are asserted. While CS is de-asserted these lines are placed in a high impedance state.

On power-up, the data bus is configured for 8 bit transfers. The data bus may be reconfigured for 16 bit by programming Master Mode register Bit 13. If D8-15 are not used they should be pulled up.

!CS (Chip Select Input)
The chip select line is an active low I/O control signal used to enable the device for read and write operations.

!WR (Write Input)
The write line is an active low I/O control signal which is used to transfer information from the data bus to one of the internal command or data registers.

!RD (Read Input)
The read line is an active low I/O control signal which is used to transfer information from one of the internal data or command registers to the data bus.

C/!D (Control/Data Port Select Input)
The C/D line is used in conjunction with the CS, RD, and WR to select which internal command or data register is being written to or read from. The C/D line selects between the command and data register sets as summarized in Table 3

EXTENDED I/O SIGNALS

The following signals are extensions to the original AM9513 device and are available only in the PQFP-100 package. The DIP-40 and PLCC-44 packaged devices will operate normally in their absence.

!INT 1-5 (Interrupt Outputs - PQFP-100 pkg only)
The interrupt lines are associated with individual counter outputs and may be used to generate system interrupts on the terminal count of a counter. The interrupt lines are asserted as either a pulse or level on the terminal count of a counter. Output polarity of the interrupt may be individually programmed for

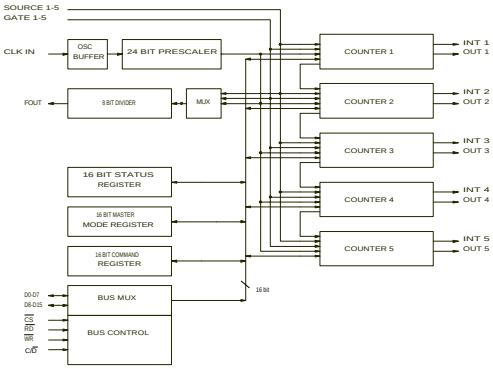


Figure 4 - CTS9513 Counter Block Diagram

each counter. Level asserted interrupt lines must be cleared with an extended set software command.

!OUTEN (Output Enable - PQFP-100 pkg only)
The Output enable line is an active low hardware override to place all timer outputs in a high impedance state. Acting directly on the counter outputs, this line allows the user to inhibit the outputs while the counters remain active.

FUNCTIONAL DESCRIPTION

SYSTEM LEVEL

The CTS9513 is addressed by the external system as two address locations. Counter and command data are written to individual counters through a sequence of indirectly addressing the internal command or data register through the command port address, followed by a write to the data port address which points to the indirectly addressed register location. Data is transferred through either two 8 bit transfers or a single 16 bit transfer. Pointer sequencing for 8 bit transfers is automatic and is transferred as least significant byte first, most significant byte second.

Rapid programming of the CTS9513 may be accomplished by use of the auto-increment feature of the data pointer. This feature is enabled by setting Master Mode Register bit 14 (MM14). When enabled, the data pointer may be sequenced through a single counter group, all counter group registers, all counter group Hold registers only, or just the control group registers.

INTERNAL CONFIGURATION

Overview
A simplified block diagram of the CTS9513 is shown in Figure 4. This diagram shows the major device elements consisting of the five counter groups, internal frequency prescaler which divides down the primary external clock source from clock input X1, the external FOUT clock prescalers which provide prescaled or divided outputs from a variety of sources, the Bus interface, Master mode register and the status register. Not shown are the extended set registers, power-on reset circuitry or internal control lines. The counter group block diagrams are shown in Figures 5 and 6. Counter groups 1 and 2 as shown in Figure 5 have an additional programmable alarm register and 16 bit comparator for implementation of time-of-day and alarm functions.

CS	RD	WR	C/D	Dx
1	X	X	X	High Impedance
0	0	1	0	Read Data
0	0	1	1	Read Command
0	1	0	0	Write Data
0	1	0	1	Write Command
0	0	0	X	Illegal

Table 3 - CTS9513 Bus Control Line States

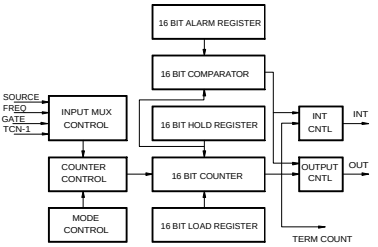


Figure 5 - CTS9513 Counter Groups 1 & 2

Counter Groups
All of the counter groups have a 16 bit counter and four programmable registers. The primary and auxiliary counter mode register controls the count source, gating and counting modes, input and output polarities, binary or BCD counting and other parameters.

Load Register
The Load register is the primary register used for storing count-up or count-down values which may be automatically reloaded into the counter for repetitive counting.

Hold Register
The Hold register may be used for storing the instantaneous count value without disturbing the count process for reading by the host system. It may also be used in certain count modes for storing alternate count values and alternately counting the load and hold register values to generate complex waveforms.

Counter Outputs
Each of the counters has a single dedicated output pin which is programmable for polarity, tri-state, low-Z to ground and a variety of output modes as described later. In addition to the output pin, the CTS9513 adds an additional dedicated interrupt output pin. This allows the timer output to produce an interrupt signal and a complex output waveform simultaneously. The Interrupt output pin may be programmed for either polarity and for a pulsed or latched level output. It is asserted each time the counter reaches TC. The level interrupt output is cleared by software control upon acknowledging the interrupt. This flexibility allows operation in a variety of bus and processor architectures.

Source Inputs
Each counter group may be programmed for a variety of count sources including any of the five source input lines, any of the internal prescaler outputs or the output of the previous counter, allowing counter concatenation and FOUT divided outputs.

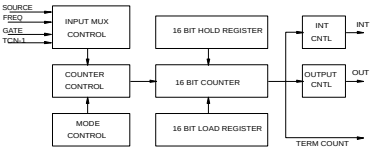


Figure 6 - CTS9513 Counter Groups 3 - 5

Gate Inputs
Gate inputs are used for external hardware triggering or synchronization of the counters. Each counter may be programmed to be gated from its own gate line or the gate lines from the previous or next counter. The gate lines may also be programmed to be level or edge sensitive and respond to active high or low signals.

The gate line may be used to either initiate one or more count sequences or used as a count enable line, allowing the counter to count only while the gate line is held active. Another mode allows the counter to be reloaded from the load or hold register depending on the state of the gate line, allowing dual frequency generation for FSK applications or similar functions.

PROGRAMMING

REGISTER PROGRAMMING

Data Bus Operation
Table 3 summarizes the I/O control signal and data status during bus reads and writes to the CTS9513. The interface control logic assumes that

- RD and WR are never active simultaneously
- RD, WR, C/D are ignored unless CS is asserted.

Register Programming
Accessing and writing to a specific data or command register from the data port is as follows.

Set Data Pointer

1. Select the appropriate data pointer value to access the desired register (example Counter group 1 Mode register 0x01)
2. Write LOAD DATA POINTER command to primary command address (write 0x0001 to device address 0x01) to set data pointer to Counter Group 1 Mode register.

This points the data port to the Group 1 mode register and set the word pointer to 1 indicating a least significant word is expected.

WRITING TO REGISTERS

Write Data to Register

1 If the 16 bit transfer mode is selected, the next write to the Primary Data Port (Device Address 0x00) will write data to the Counter mode register.
2 If the 8 bit transfer mode is selected, the next write to the Primary Data Port Address will expect the least significant word of the register value, followed by a write of the most significant word to the data port. The internal word pointer is automatically incremented.
3 If an automatic sequence command has been given the data pointer will automatically be sequenced to the next register.

READING REGISTERS

Reading from a device register follows the write sequence very closely, requiring a write to the command register to set the appropriate data pointer, followed by a read or reads from the data port. Several items should be noted when reading from the device registers:

1 The data pointer should always be reloaded before reading from the data port if the prior command was anything but a LOAD DATA POINTER command in order to update the Read data prefetch latch.
2 A LOAD DATA POINTER command should be issued to the device prior to reading a HOLD register following a hardware triggered SAVE of the counter contents to the HOLD register.

COMMANDS

COUNTER COMMANDS

Counter commands are divided into two main groups. Those commands which directly affect counter operation, often shortcuts to programming specific register functions, and those associated with indirectly addressing the counters'internal registers.

Counter control commands can be further subdivided into those commands which affect individual counter operation and those which affect the overall device operation.

Table 4 Lists the commands associated with indirect addressing of the counter internal registers. These commands point the data port to the appropriate internal register in order to read or write to them.

Table 5 Lists the commands associated with controlling the actions of individual counters. They are made up basically of the ARM, DISARM, LOAD, SAVE, CLEAR, SET and STEP commands.

ARM Command
A counter must be ARMed before it can commence counting. Once ARMed, a counter may be programmed to begin counting immediately or to await a hardware trigger to initiate counting.

DISARM Command
The DISARM command halts and disables any further counting regardless of any hardware gating or triggering. While DISARMed a counter may be reloaded, SAVEd or incremented or decremented using the STEP Command

LOAD Command
The LOAD command is used to load the counter with the value stored in either the associated Load or Hold register. It may also serve as an automatic retrigger of the counter once the counter is loaded.

C7	C6	C5	C4	C3	C2	C1	C0	Command Register Bit
0	0	0	E2	E1	G4	G2	G1	Load Data Pointer Commands
								G1-4 Group Pointer
								E1-2 Element Pointer
0	0	0	0	0	0	0	0	(Originally Reserved)
0	0	0	0	0	0	0	1	Counter 1 Mode Register
0	0	0	0	0	0	1	0	Counter 2 Mode Register
0	0	0	0	0	0	1	1	Counter 3 Mode Register
0	0	0	0	0	1	0	0	Counter 4 Mode Register
0	0	0	0	0	1	0	1	Counter 5 Mode Register
0	0	0	0	0	1	1	0	Counter 1 Aux Mode (Originally Reserved)
0	0	0	0	0	1	1	1	Alarm Register 1 / Control Cycle
0	0	0	0	1	0	0	0	Counter 2 Aux Mode (Originally Reserved)
0	0	0	0	1	0	0	1	Counter 1 Load Register
0	0	0	0	1	0	1	0	Counter 2 Load Register
0	0	0	0	1	0	1	1	Counter 3 Load Register
0	0	0	0	1	1	0	0	Counter 4 Load Register
0	0	0	0	1	1	0	1	Counter 5 Load Register
0	0	0	0	1	1	1	0	Counter 3 Aux Mode (Originally Reserved)
0	0	0	0	1	1	1	1	Alarm Register 2 / Control Cycle
0	0	0	1	0	0	0	0	Counter 4 Aux Mode (Originally Reserved)
0	0	0	1	0	0	0	1	Counter 1 Hold Register
0	0	0	1	0	0	1	0	Counter 2 Hold Register
0	0	0	1	0	0	1	1	Counter 3 Hold Register
0	0	0	1	0	1	0	0	Counter 4 Hold Register
0	0	0	1	0	1	0	1	Counter 5 Hold Register
0	0	0	1	0	1	1	0	Counter 5 Aux Mode (Originally Reserved)
0	0	0	1	0	1	1	1	Master Mode Register / Control Cycle
0	0	0	1	1	0	0	0	Aux Master Mode (Originally Reserved)
0	0	0	1	1	0	0	1	Hold Register Cycle
0	0	0	1	1	0	1	0	Hold Register Cycle
0	0	0	1	1	0	1	1	Hold Register Cycle
0	0	0	1	1	1	0	0	Hold Register Cycle
0	0	0	1	1	1	0	1	Hold Register Cycle
0	0	0	1	1	1	1	0	(Originally Reserved)
0	0	0	1	1	1	1	1	Status Register

Table 4 - CTS9513 Data Pointer Commands

SAVE Command
The SAVE command is used to save the contents of the counter while counting continues. This allows the counter value to be read without interfering with the counter. Subsequent SAVE commands will overwrite any previous contents of the Hold register.

CLEAR Command
The CLEAR command is used to reset the counter output toggle to initialize it to a low state. This command is only active if the output toggle is programmed. It is inactive if a Terminal Count output is specified.

SET Command
The SET command is used to set the counter output toggle to initialize it to a high state. This command is only active if the output toggle is programmed. It is inactive if a Terminal Count output is specified.

STEP Command
The STEP Command increments of decrements the selected counter by one depending on the operating mode.

Master Mode Commands
A number of commands directly affect the Master Mode Register without having to write to it directly. These commands affect primarily the modes of the data path, data pointer sequencing, enabling the divided FOUT output clocks and clearing of latched interrupt outputs from the counters. Table 6 summarizes thes commands

REGISTER DEFINITIONS

STATUS REGISTER

The 16 bit Status Register indicates the
1 Status of the internal word pointer
2 Status of the counter outputs
3 Status of the counter interrupt outputs

When reporting the status of the counter output, the status bit reflects the exact state of the output pin, regardless of how the output pin state or toggle is programmed.

When an output low impedance to ground output is programmed, the Status bit reflects and Active High status. When the output is programmed for a high impedance output or is externally inhibited, the status register reflects an active low output. Table 7 summarizes the status register bit assignments.

Master Mode Commands
The Master Mode registers are 16 bit read/Write registers used to set counter parameters not associated with individual counters. These parameters include setting the data bus width, prescaling factors, Time of day functions and data pointer sequencing. The primary Master Mode Register is identical in function to the original 9513 device. The auxiliary Master Mode Register is used to program extended features of the CTS9513. If the auxiliary register is not programmed the device behaves as an original 9513 device. Table 8 summarizes the primary and auxiliary Master Mode Register bit assignments.

On Power-up the Master Mode register is cleared to all zeros resulting in the following default conditions:
1 Time of Day disabled
2 Alarm Comparators Disabled
3 FOUT source is F1
4 FOUT divider set for divide by 16
5 FOUT enabled
6 Data Bus 8 bits
7 Data Pointer Sequencing enabled
8 Frequency scaling Binary

C7	C6	C5	C4	C3	C2	C1	C0	Command Register Bit
			S5	**S4**	**S3**	**S2**	**S1**	**S1-5 - Counter Group Select**
0	0	1	S5	S4	S3	S2	S1	Arm Selected Counters
0	1	0	S5	S4	S3	S2	S1	Load Selected Counters
0	1	1	S5	S4	S3	S2	S1	Load and Arm Selected Counters
1	0	0	S5	S4	S3	S2	S1	Disarm and Save Selected Counters
1	0	1	S5	S4	S3	S2	S1	Save selected counters to Hold Registers
1	1	0	S5	S4	S3	S2	S1	Disarm Selected Counters
					N4	**N2**	**N1**	**N1-4 Counter Group Select (001 = N = 101**
1	1	1	0	0	N4	N2	N1	Clear Selected Counter Toggle Out
1	1	1	0	1	N4	N2	N1	Set Selected Counter Toggle Out
1	1	1	1	0	N4	N2	N1	Step Selected Counter (up/down by CM3)

Table 5 - Counter Action Related Commands

C7	C6	C5	C4	C3	C2	C1	C0	Command Register Bit
1	1	1	0	0	0	0	0	Clear MM14 (Enable Data Pointer Sequencing)
1	1	1	0	0	1	1	0	Clear MM12 (FOUT Gate On)
1	1	1	0	0	1	1	1	Clear MM13 (Enable 8 bit Bus Mode)
1	1	1	0	1	0	0	0	Set MM14 (Disable Data Pointer Sequencing)
1	1	1	0	1	1	1	0	Set MM12 (FOUT Gate Off)
1	1	1	0	1	1	1	1	Set MM13 (Enable 16 bit Bus Mode)
1	1	1	1	0	0	0	0	**(Originally Reserved)**
1	1	1	1	0	1	1	0	**(Originally Reserved)**
1	1	1	1	0	1	1	1	**Clear All Interrupts (Orig Reserved)**
1	1	1	1	1	0	0	0	Enable Write Pre-Fetch
1	1	1	1	1	0	0	1	Disable Write Pre-Fetch
1	1	1	1	1	0	1	0	**Clear Counter 1 Interrupt (Orig Reserved)**
1	1	1	1	1	0	1	1	**Clear Counter 2 Interrupt (Orig Reserved)**
1	1	1	1	1	1	0	0	**Clear Counter 3 Interrupt (Orig Reserved)**
1	1	1	1	1	1	0	1	**Clear Counter 4 Interrupt (Orig Reserved)**
1	1	1	1	1	1	1	0	**Clear Counter 5 Interrupt (Orig Reserved)**
1	1	1	1	1	1	1	1	Master Reset

Table 6 - Device Level Commands

S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
RSVD	RSVD	OUTEN	INT5	INT4	INT3	INT2	INT1	CMP2	CMP1	OUT5	OUT4	OUT3	OUT2	OUT1	WP
RESERVED		Output Enable Status	Interrupt Status Reflects actual state of Interrupt Output					Comparator Status		Counter Output Status Reflects Actual State of Output Prior to Tri-State Buffer					Byte Pointer

Table 7 - Status Register

Time of Day (Bits MM0-1)
Bits MM0 and MM1 control the Time-of-day functions for counters 1 and 2. When enabled, additional counter logic is enabled to allow the two counters to operate as a 24 hour clock.
Counters 1 and two must be programmed for BCD counting. To initialize the time, appropriate values are loaded in the Counter Load registers. To read the time a SAVE command is issued to Counters 1 and 2 and the values read from the Hold registers.

Table 9 illustrates the Time-of-day storage configuration. In short, Counter 2 bits 8-15 form a two digit BCD Hours counter, Bits 0-7 form a two digit BCD Minutes counter. Counter 1 bits Bits 8-15 form a two digit BCD seconds counter, Bits 4-7 form a tenth second counter and Bits 0-3 form a division factor for the input source for divide by 5, 6 or 10.

Comparator Enable (Bits MM2-3)

The two 16 bit comparators on counters 1 and 2 may be used in any mode. When enabled, the output of the comparators are routed to the output of the counter. The output will be asserted when the comparison between the counter and alarm register contents are true. It will remain asserted as long as the counter and alarm register remain the same.
In the Time-of-Day mode the comparators operate in conjunction such that the output of the counter 2 comparator is asserted only when both comparators 1 and 2 are true. the comparator 1 output will continue to operate normally.

FOUT Source (Bits MM4-7)
Fifteen different sources may be routed to the input of the FOUT divider, including the five SOURCE inputs, five GATE inputs and five of the internal divided frequencies derived from the X1 input. Additional Sources may be programmed using the extended Master mode register functions.

FOUT1 Divider (Bits MM8-11)
FOUT may be divided by 1 to 256. Master mode bits MM8-11 allow programming of the FOUT divider from 1 to 16 inclusive. Higher order division factors are programmed through the extended Master Mode register functions.

AMM15	AMM14	AMM13	AMM12	AMM11	AMM10	AMM9	AMM8	AMM7	AMM6	AMM5	AMM4	AMM3	AMM2	AMM1	AMM0
RSRVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	DIV1-32 Ext FOUT Source and Divider Bits	DIV1-16	FOUT1-16

MM15	MM14	MM13	MM12	MM11	MM10	MM9	MM8	MM7	MM6	MM5	MM4	MM3	MM2	MM1	MM0
SCALE	POINT	BUS	FGATE1	DIV1-8	DIV1-4	DIV1-2	DIV1-1	FOUT1-8	FOUT1-4	FOUT1-2	FOUT1-1	COMP2	COMP1	TOD2	TOD1
Scale Mode 0 = Binary 1 = BCD	Data Pointer 0 = Enable 1 = Dis-able	Data Bus Width 0 = 8 1 = 16	FOUT Mode 0 = On 1 = Off	FOUT Divider (Including AMM1-2) 000000 = Divide by 16 000001 = Divide by 1 000010 = Divide by 2 000011 = Divide by 3 000100 = Divide by 4 000101 = Divide by 5 . . . . 111110 = Divide by 62 111111 = Divide by 63				FOUT Source Select (With AMM0) 00000 = F1 00001 = Source 1 00010 = Source 2 00011 = Source 3 00100 = Source 4 00101 = Source 5 00110 = Gate 1 00111 = Gate 2 01000 = Gate 3 01001 = Gate 4 01010 = Gate 5 01011 = F1 01100 = F2 01101 = F3 01110 = F4 01111 = F5 10000 = F6 10001 = F7 10010 = FOUT 2 10011 - 11111 = Reserved				Comparator Mode 00 = Disabled 01 = Comparator 1 On 10 = Comparator 2 On 11 = Both On		Time of Day Mode 00 = TOD Disabled 01 = TOD Enabled /5 10 = TOD Enabled /6 11 = TOD Enabled /10	

Table 8 - Master and Auxiliary Master Mode Register Definitions

C2-15	C2-14	C2-13	C2-12	C2-11	C2-10	C2-9	C2-8	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	C2-0
10's Hours				Hours				10's Minutes				Minutes			
BCD DATA 0 - 23 Hours								BCD DATA 0-59 Minutes							

C1-15	C1-14	C1-13	C1-12	C1-11	C1-10	C1-9	C1-8	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	C1-0
10's Seconds				Seconds				10th Seconds				Division Factor (5, 6, 10)			
BCD DATA 0.0 - 59.9 Seconds															

Table 9 - CTS9513 Time-of-Day Data Format

FOUT Enable (Bit MM12)
The FOUT output may be enabled or disabled and placed in a low impedance state to ground under software control.

Bus Width (Bit MM13)
When set, this bit places the device into a 16 bit external data bus mode. When cleared, the external data bus is set to 8 bits and registers are loaded 8 bits at a time, least significant word first.

Data Pointer Sequencing (Bit MM14)
When cleared, this bit enables automatic sequencing of the data pointer as defined by the data pointer commands. When set, the data pointer contents may only be changed by command.

Scaling (Bit MM15)
This bit determines whether the internal frequency prescaler operates as a BCD or Binary Divider. Figure 6 illustrates the internal 24 bit prescaler and its outputs.

COUNTER REGISTERS

Load Register
The load register is a read/write counter register used to store the counter initial value. The load register value can be transferred into the counter each time the counter reaches a "terminal count." A "terminal count" is defined as that period of time the counter value would have been zero if an external value had not been transferred into the counter. In all operating modes the value in either the load or hold register is transferred into the counter when the counter reaches terminal count.

Hold Register
The hold register is a read /write dual purpose register. In some operating modes the hold register may be used to store counter instantaneous values on command without disturbing the counter action for readout by the host. Other operating modes allow the hold register to be used as storage for counter values in a fashion similar to the Load register. The counter may be loaded from the Hold register at terminal count, or alternately loaded from the Load and Hold register at terminal count.

Alarm Register
Counters 1 and 2 contain an additional 16 bit Alarm register and corresponding 16 bit comparator. When the value in the counter matches the value stored in the Alarm register the output pin for the counter goes true. The output remains true as long as the counter value matches the Alarm register value. The output may be programmed for active high or active low by the counter mode register.

COUNTER MODE REGISTER

Each counter group contains a mode control register which controls the counter behavior, gating and output active states and polarities and counter source. The counter mode register is initialized at power-up to all zeroes. This translates to an initial counter mode of:

1 Output Low impedance to Ground
2 Count Down
3 Count Binary
4 Count Once
5 Load Register Selected
6 No Retriggering
7 F1 source selected
8 Positive-true input polarity
9 No Gating

The Counter Mode Register must be loaded while the counter is disarmed.. Table 10 summarizes the Counter Mode Register bit assignments.

Output Control (Bits CM0-2)
The counter output may be configured to be disabled, programmed to follow the counter terminal count or to toggle its state at each terminal count. The output logic for each counter is shown in Figure 8.

CM31	CM30	CM29	CM28	CM27	CM26	CM25	CM24	CM23	CM22	CM21	CM20	CM19	CM18	CM17	CM16
RESERVED													**IPOL**	**IMODE**	**SRC1-16**
													Interrupt Polarity 0 = Low 1 = High	Interrupt Mode 0 = Pulse 1 = Latch	

COUNTER MODE REGISTER - LOW WORD

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
GCTL3	GCTL2	GCTL1	EDGE	SRC1-8	SRC1-4	SRC1-2	SRC1-1	GATE	RELOAD	REPEAT	COUNT	DIR	OUT4	OUT2	OUT1
Gate Control 000 = No Gating 001 = Active High, TC N-1 010 = Active High Level GateN+1 011 = Active High Level GateN-1 100 = Active High Level GateN 101 = Active Low Level GateN 110 = Active High Edge GateN 111 = Active Low Edge GateN			**Edge Mode** 0 = Rising 1 = Falling	**Count Source Selection (With CM16)** 00000 = TC N-1 00001 = Source 1 00010 = Source 2 00011 = Source 3 00100 = Source 4 00101 = Source 5 00110 = Gate 1 00111 = Gate 2 01000 = Gate 3 01001 = Gate 4 01010 = Gate 5 01011 = F1 01100 = F2 01101 = F3 01110 = F4 01111 = F5 10000 = F6 10001 = F7 10010 = FOUT 1 10011 = FOUT 2 10100 - 11111 = RESERVED			**Gate Mode** 0 = Off 1 = On	**Reload Mode** 0 = Load 1 = Both	**Repeat Mode** 0 = once 1 = repeat	**Count Mode** 0 = Binary 1 = BCD	**Count Direction** 0 = Down 1 = Up	**Output Control** 000 = Inactive, Output Low 001 = Active High on TC 010 = TC Toggled 011 = Illegal 100 = Inactive, Output High Z 101 = Active Low on TC 110 = Illegal *111 = Illegal		

Table 10 - CTS9513 Counter Mode and Auxiliary Counter Mode Register Bit Assignments

The output may be disabled by either placing it in a high impedance state or in a low impedance state to ground. The outputs may also be hardware inhibited with the line.

In the Terminal count mode, the output may be programmed to output an active high or active low pulse which is equal to one count source clock period.

In the output toggle mode, the output changes state whenever the counter reaches a terminal count. The output state may be initialized with the SET and CLEAR counter commands.

Count Control (Bits CM3-7)

Whenever the counter reaches a TC, the counter automatically reloads the counter from the Load or Hold Register. Which register the counter loads from, whether the counter counts repeatedly or once, whether the counter counts binary or BCD and whether the counter is under hardware control is controlled by the Count control.

Bit CM3 controls whether the counter counts in Binary or BCD fashion. Bit CM4 determines whether the counter counts up or down. Bit CM5 determines whether the counter counts once and disarms itself, or will continue counting and reloading the counter

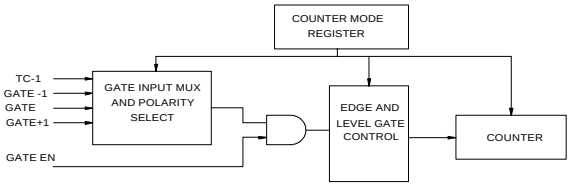


Figure 9 - CTS9513 Counter Gating Input Logic Block Diagram

until commanded to disarm.

Bit CM6 determines the source from which the counter will be reloaded. The actions of CM6 depend on the gating control settings. If CM6 is cleared, the counter reloads from the Load Register at TC. If CM6 is set, the counter may reload from either the Load or the hold register depending on the gating mode. It may alternate with the Load register or be controlled from the gate to reload from the load or hold register.

Bit CM7 controls whether hardware retriggering of the counter is enabled. Its actions depend on the settings of CM5, CM6 and the gating controls.

If some type of gating is enabled and CM7 is cleared, hardware retriggering is disabled. When CM7 is set, hardware retriggering is enabled and the counter is retriggered any time an active gate edge is received. When retriggered the counter value is saved in the Hold register and the counter reloaded from the Load register.

If no gating is enabled and CM7 is cleared, the gate input has no effect on counting. If CM7 is set then the Gate input controls whether the counter is reloaded from the Load or Hold Register.

Count Source (Bits CM8-12)
The count source determines which source is used as an input to the counter. There are 20 possible count sources, 16 of which may be selected with bits CM8-12. Additional Count sources may be specified with the extended registers. Figure 8 illustrates the internal 24 bit prescaler whose outputs may be used as count sources.

Gating Control (Bits CM13-15)
Gating control determines whether the counter is hardware gated or not. When gating is disabled the counter will continue as long as the counter is armed. If any gating mode is enabled the counter action is determined by some hardware gate condition.

Gating of the counter may be controlled from the gate line associated with the counter or gate lines associated with adjacent counters. Gating on the line associated with the counter may be programmed for edge or level sensitive, active high or active low. The counter may also be gated by the TC output of the previous counter. The gating control logic is outlined in Figure 7.

COUNTER MODES

Counter modes continue as in the 9513 to retain their mode designations A-X, with modes M, P, T, U and V reserved. Tables 11-12 summarize the counter modes and the associated settings of the counter mode bits CM5-7 and CM13-15.

Figures 10 through 28 illustrate the counter modes. All representative waveforms assume counting down on rising source edges. A TC mode and Toggled

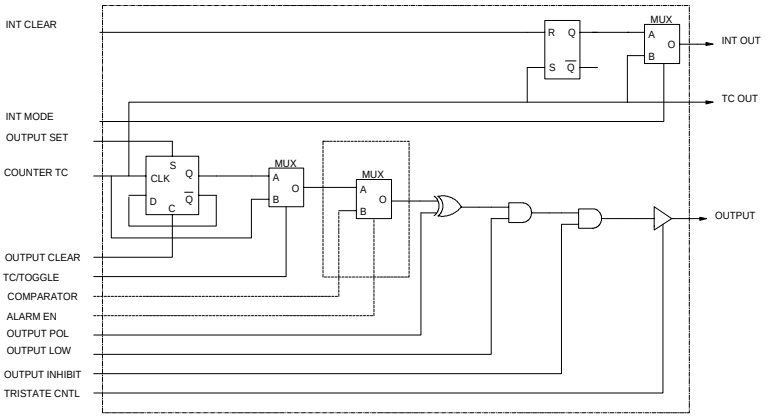
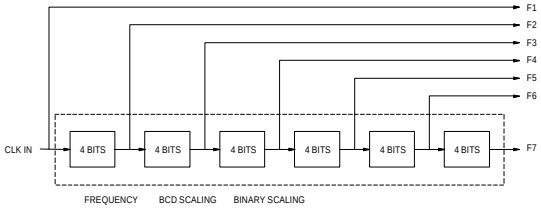


Figure 7 - CTS9513 Counter Output Logic Block Diagram



FREQUENCY	BCD SCALING	BINARY SCALING
F1	CLK IN	CLK IN
F2	CLK / 10	CLK / 16
F3	CLK / 100	CLK / 256
F4	CLK / 1000	CLK / 4096
F5	CLK / 10000	CLK / 65536
F6	CLK / 100000	CLK / 1048576
F7	CLK / 1000000	CLK / 16777216

Figure 8 - CTS9513 Counter Internal Prescaler Block Diagram

output waveform are shown in each waveform. For waveforms which disarm automatically on TC the software ARM command is shown in conjunction with a Write pulse. Repetitive waveforms do not show the write pulse or ARM command. The letters L and H are used in the figures to denote Load and Hold register values and the letters K and N to denote arbitrary counter values.

In all cases, the counter begins counting on the first count source edge following the Write pulse in software triggered modes and the first source edge following a valid gate edge in hardware triggered or enabled modes.
In gate controlled modes which inhibit counting, the counter is suspended for any valid source edges that occur after de-assertion of the gate line.

OPERATING MODE	A	B	C	D	E	F	G	H	I	J	K	L
CM7 (SPECIAL GATE)	0	0	0	0	0	0	0	0	0	0	0	0
CM6 (RELOAD SOURCE)	0	0	0	0	0	0	1	1	1	1	1	1
CM5 (REPITITION)	0	0	0	1	1	1	0	0	0	1	1	1
CM13-15 (GATE CONTROL)	000	LVL	EDG	000	LVL	EDG	000	LVL	EGD	000	LVL	EDG
Count to TC Once	X	X	X									
Count to TC Twice							X	X	X			
Count to TC repeatedly				X	X	X				X	X	X
Gate Input Inactive	x			x			x			x		
Count while gate active		x			x			x			x	
Count once on gate edge			x			x						
Count twice on gate edge									x			x
No Hardware retriggering	x	x	x	x	x	x	x	x	x	x	x	x
Reload from Load on TC	x	x	x	x	x	x						
Alternate Load/Hold on TC							x	x	x	x	x	x
Gate Controlled Load/Hold												
Gate Retrigger Counter												

Table 11 - Counter Modes A-L

OPERATING MODE	M	N	O	P	Q	R	S	T	U	V	W	X
CM7 (SPECIAL GATE)	1	1	1	1	1	1	1	1	1	1	1	1
CM6 (RELOAD SOURCE)	0	0	0	0	0	0	1	1	1	1	1	1
CM5 (REPITITION)	0	0	0	1	1	1	0	0	0	1	1	1
CM13-15 (GATE CONTROL)	000	LVL	EDG	000	LVL	EDG	000	LVL	EGD	000	LVL	EDG
Count to TC Once		X	X									
Count to TC Twice							X					
Count to TC repeatedly					X	X				X		
Gate Input Inactive							X			X		
Count while gate active		X			X							
Count once on gate edge			X			X						
Count twice on gate edge												
No Hardware retriggering							X			X		
Reload from Load on TC		X	X		X	X						
Alternate Load/Hold on TC												
Gate Controlled Load/Hold							X			X		
Gate Retrigger Counter		X	X		X	X						

Table 12 - Counter Modes M-X

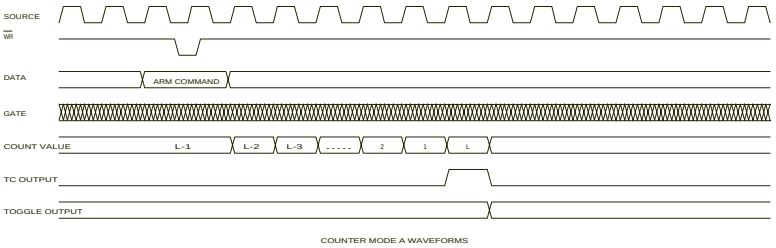


Figure 10 - CTS9513 Counter Mode A Representative Waveforms

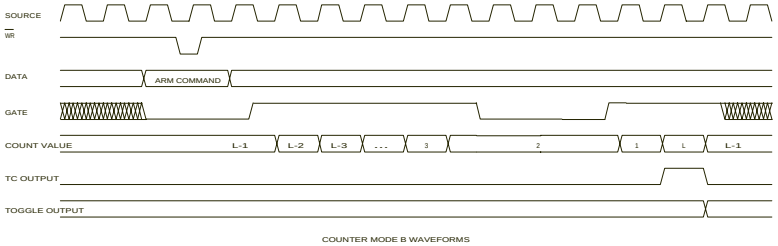


Figure 11 - CTS9513 Counter Mode B Representative Waveforms

MODE A - SOFTWARE TRIGGERED STROBE WITH NO GATING

As shown in Figure 10, The counter is only active after receipt of an ARM command. On reaching TC the counter automatically reloads from the Load register and disarms, awaiting the next software ARM command.

MODE B - SOFTWARE TRIGGERED STROBE WITH LEVEL GATING

In Mode B, illustrated in Figure 11 the counter is only active when both an ARM command has been received and the selected Gate line is active. The counter will halt counting when the gate line is de-asserted and resume counting when the gate line is re-asserted until the counter reaches TC. When the counter reaches TC the timer will reload from the load register and disarm automatically until a new ARM command is received.

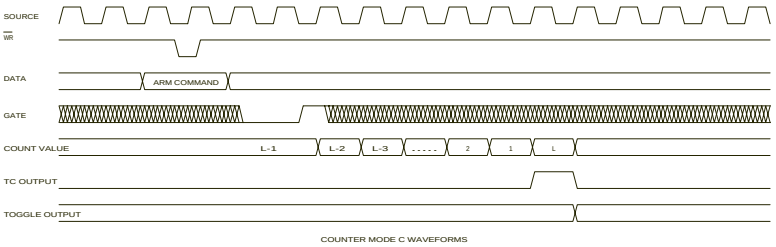


Figure 12 - CTS9513 Counter Mode C Representative Waveforms

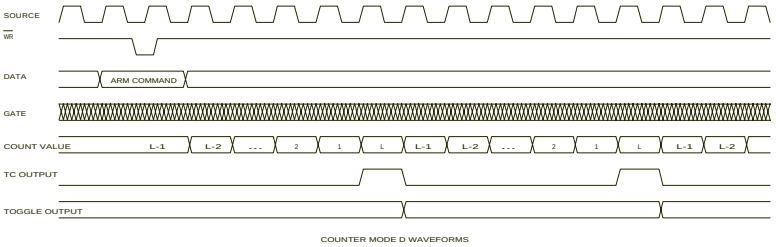


Figure 13 - CTS9513 Counter Mode D Representative Waveforms

MODE C HARDWARE TRIGGERED STROBE

In Mode C, as shown in Figure 12, the counter is active only after receipt of an ARM command and the application of a Gate edge to the selected gate line. Once a Gate edge is sensed, the counter will count until it reaches TC. Subsequent gate actions have no further effect on the counter action. The counter will remain inactive until receipt of a new ARM command and Gate.

MODE D RATE GENERATOR WITH NO HARDWARE GATING

Mode D, illustrated in Figure 13. is commonly used as a programmable frequency source as it continues to count repetitively until receipt of a DISARM command. Once ARMed, the counter counts to TC, automatically reloads the counter from the Load register and begins counting again. The waveform produced can be a square wave if the Toggle output mode is specified. The Gate line has no effect on the counter action.

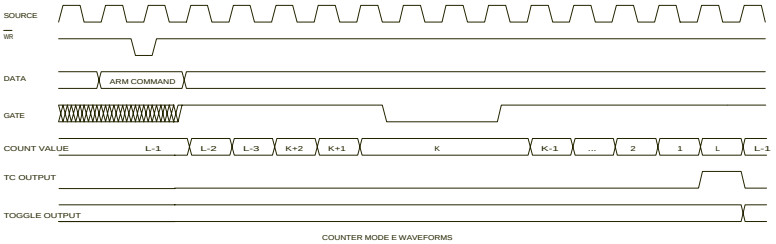


Figure 14 - CTS9513 Counter Mode E Representative Waveforms

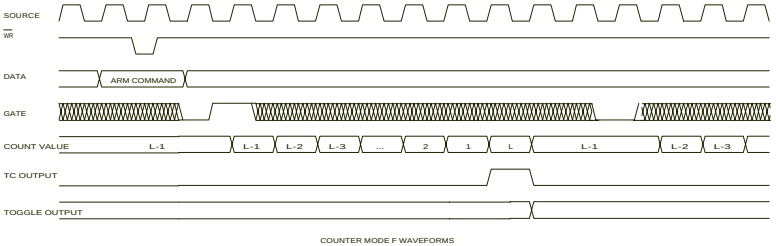


Figure 15 - CTS9513 Counter Mode F Representative Waveforms

Mode E Rate Generator with Level Gating

Mode E is similar to Mode D in that the counter will count repetitively after being ARMed and as long as the selected Gate line is asserted. As shown in Figure 14, this allows gating of the pulse train or square wave on and off from an external source via the gate line.

Mode F Non-Retriggerable One Shot

Mode F is similar to Mode C with the exception that the counter may be retriggered without receipt of a new ARM Command. As shown in Figure 15, Once the counter has been ARMed, and a valid Gate edge has been received, the counter will count once to TC and reload the counter from the Load register. It will remain inactive until receipt of another Gate edge. While counting, subsequent gate edges are disregarded.

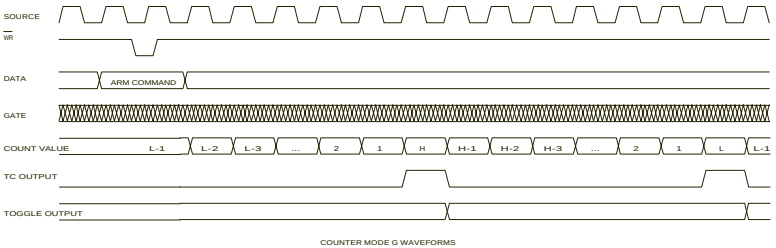


Figure 16 - CTS9513 Counter Mode G Representative Waveforms

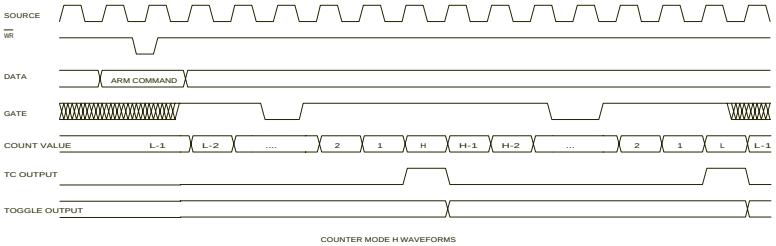


Figure 17 - CTS9513 Counter Mode H Representative Waveforms

MODE G SOFTWARE TRIGGERED DELAYED PULSE ONE-SHOT

In Mode G, once the counter has been ARMed, the counter will:

1. Count to TC with the Load register value
2. Reload itself automatically from the Hold Register.
3. Count to TC with the Hold Register Value
4. Disarm itself and reload the counter with the Load register Value.

This produces a waveform as illustrated in Figure 16 in which the counter can in TC mode produce a pair of pulses with the first pulse delay controlled by the Load count value and the delay between the pulses determined by the Hold register count.

If the Toggle Output mode is selected, the output produced is a pulse width determined by the Hold count and an initial delay determined by the Load count. This is the more common use of this mode of operation.

MODE H SOFTWARE TRIGGERED DELAYED PULSE ONE-SHOT WITH HARDWARE GATING

Mode H is similar to Mode G with the exception that the counter is active only after receipt of an ARM command and a valid Gate input. As shown in Figure 17 the counter counts only as long as the Gate line is asserted and suspended while the Gate line is de-asserted. Tas in Mode G the counter counts to TC using the Load register value, reloads from the hold register and counts to a second TC. Once the counter reaches the second TC the counter disarms itself and awaits another ARM command.

This mode allows extension of either the initial delay or the delayed pulse width by use of the Gate.

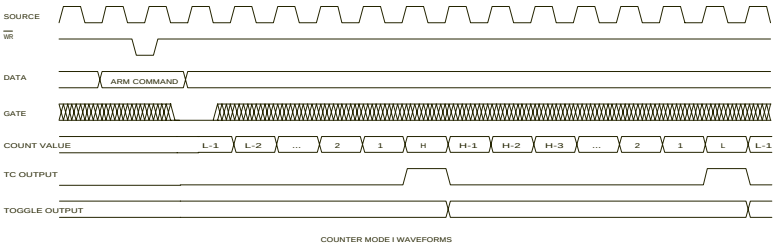


Figure 18 - CTS9513 Counter Mode I Representative Waveforms

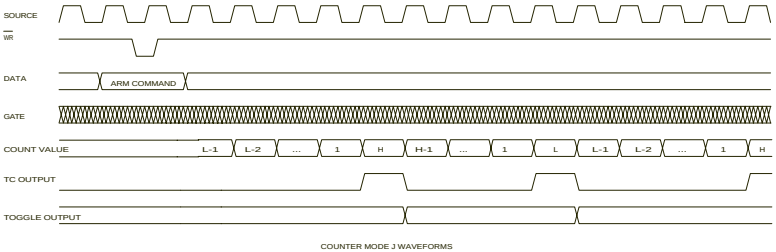


Figure 19 - CTS9513 Counter Mode J Representative Waveforms

MODE I HARDWARE TRIGGERED DELAYED PULSE STROBE

Mode I is similar to Mode G with the exception that the counter is active only after receipt of an ARM command and a valid Gate Edge. As illustrated in Figure 18, the counter will count to TC, reload from the Hold Register, count to TC then disarm itself. Once a valid Gate edge has been received the gate line has no further action on the counter.

MODE J VARIABLE DUTY CYCLE RATE GENERATOR WITH NO HARDWARE GATING

This mode is used primarily for generation of variable duty cycle waveforms. Once armed the counter will count repeatedly until disarmed. The counter will count to the first TC, reload automatically from the Hold register, count to the next TC, reload automatically from the Load register and repeat the cycle. If the toggle output mode is selected, the output will have an on(or off) time equal to the load count and off(on) time equal to the hold count. As shown in Figure 19.

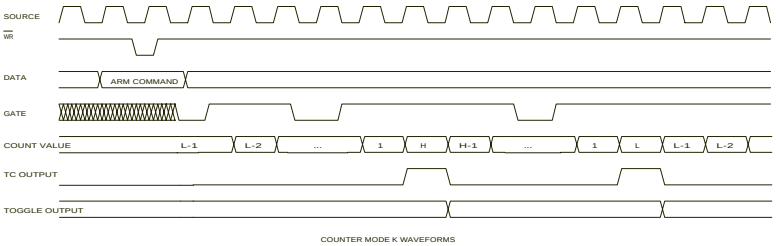


Figure 20 - CTS9513 Counter Mode K Representative Waveforms

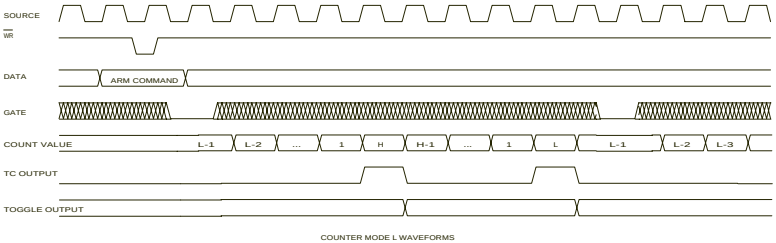


Figure 21 - CTS9513 Counter Mode L Representative Waveforms

Mode K Variable Duty Cycle Rate Generator with Level Gating

Mode K is similar to Mode J with the exception that the counter is enabled only after being ARMed and when the selected Gate line is asserted. When the Gate line is deasserted the counter stops. This allows the gate to modulate the duty cycle of either state as illustrated in Figure 20.

Mode L Hardware Triggered Delayed Pulse One-Shot

Mode L is used often as an externally triggered delayed pulse generator, where the delay and pulse width are both programmable. Like Modes J and K, the counter cycles through the load count, reloads from the hold at the first TC, and counts to the second TC.

Unlike Modes J and K, however the counter is only active after being ARMed and after a valid gate edge is received. As shown in Figure 21 the gate edge initiates one count cycle and is disregarded for the rest of the cycle. After one count cycle (Load and Hold) the counter stops until another gate edge is received.

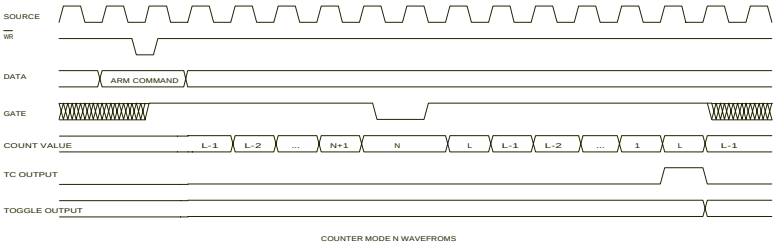


Figure 22 - CTS9513 Counter Mode N Representative Waveforms

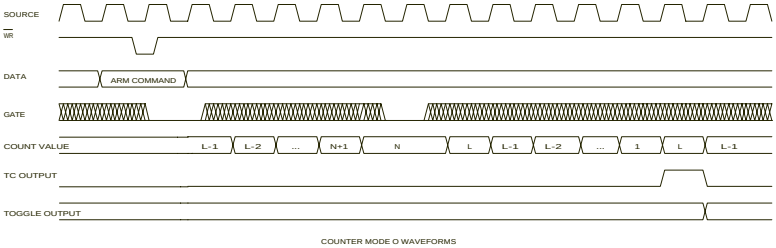


Figure 23 - CTS9513 Counter Mode O Representative Waveforms

Mode N Software Triggered Strobe with Level Gating and Hardware Retriggering

In Mode N, once ARMed, the counter is active only as long at the selected Gate line is asserted. Counting begins only after the gate line is asserted after the counter is ARMed. If the Gate line remains asserted the counter will count to TC, reload automatically from the load register and disarm itself until receipt of a new ARM command. If the gate is deasserted prior to the counter reaching TC the counter will halt. When the Gate line is reasserted on a halted counter, the count value is transferred to the Hold register and the next valid count source edge will cause the counter to reload from the Load register and begin counting again, effectively retriggering the counter as shown in Figure 22.

One application of this mode is to measure the delay between two successive gate edges by reading the remainder count value from the hold register.

Mode O Software Triggered Strobe with Edge Gating and Hardware Retriggering

Mode O is similar to Mode N in that the counter must be ARMed and a valid Gate edge must be received to start the counter. Unlike most other modes, however, each time a valid gate edge is received prior to the counter reaching TC will cause the counter to be retriggered by reloading the counter from the load register on the first valid source edge following a valid gate edge. If the counter is allowed to reach TC is automatically reloads from the Load register and disarms itself.

The counter is insensitive to gate edges while disarmed and while counting. The counter is sensitive only to a valid gate edge while counting.

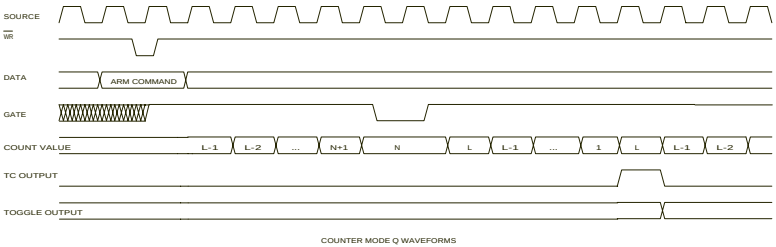


Figure 24 - CTS9513 Counter Mode Q Representative Waveforms

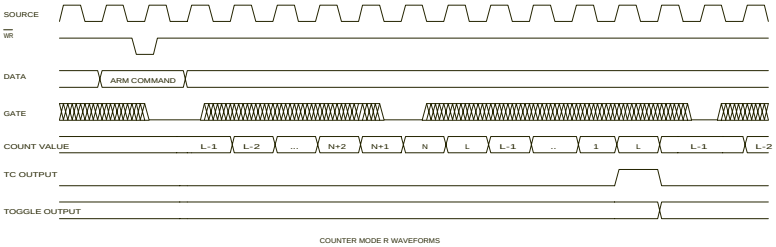


Figure 25 - CTS9513 Counter Mode R Representative Waveforms

MODE Q RATE GENERATOR WITH SYNCHRONIZATION

Mode Q provides a continuous rate generator which may be externally gated or synchronized to an external event via the Gate input. As shown in Figure 24, once an ARM command is received, the counter will continuously count to TC, reload the Load register and repeat as long as the Gate line is asserted. While the Gate line is deasserted the counter is inhibited. On the active going edge of the gate signal the counter is reloaded from the Load register, resetting the counter and resume counting on the second valid source edge following the Gate edge.

MODE R RETRIGGERABLE ONE-SHOT

Mode R, as shown in Figure 25, begins counting only after receipt of an ARM command and a valid active Gate edge. The counter will count once to TC and stop. The counter will remain inactive until receipt of a subsequent valid Gate edge.

If a valid Gate Edge is received prior to the counter reaching TC the counter value will be saved in the Hold register and the counter reloaded from the Load register, retriggering or resetting the counter. The counter in insensitive to the Gate level and gate actions do no inhibit the counter as in Mode Q.

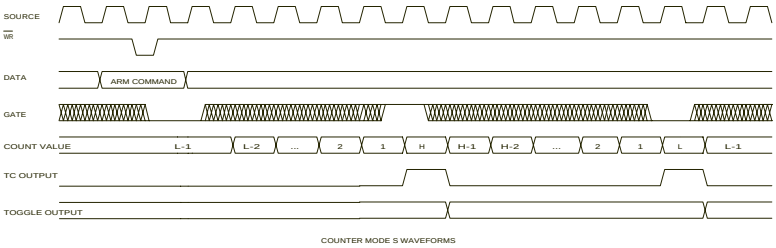


Figure 26 - CTS9513 Counter Mode S Representative Waveforms

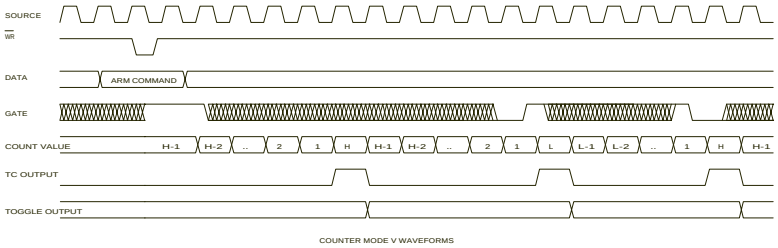


Figure 27 - CTS9513 Counter Mode V Representative Waveforms

Mode S Gate Controlled Strobe

In Mode S, once ARMed the counter will count to TC twice and disarm. During this time the State of the Gate line determines whether the counter is loaded from the Load or Hold Register. The Gate line does not affect or initiate the counter in this Mode. Its only action is a level sensitive selection of the Load or Hold Register as a counter reload source.

As shown in Figure 26, at each TC in the cycle, if the Gate line is high, the counter will be reloaded from the Hold Register. If it is Low the counter is reloaded from the Load Register.

Mode V Frequency Shift Keying

Mode V is similar to mode S in that the Gate line act to select which register the counter is reloaded from, but counts continuously once armed. If the Toggled output is used, the output may be used to switch between two frequencies determined by the Load and Hold Count values and the state of the Gate line as shown in Figure 27. This is used in Frequency Shift Keying (FSK) applications.

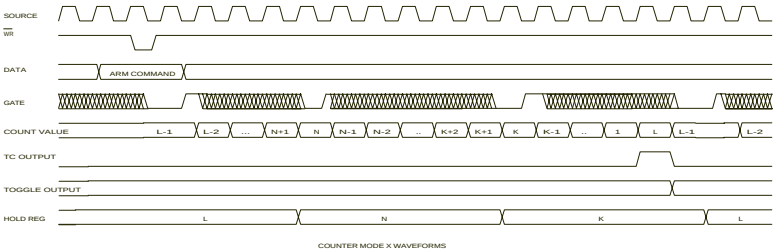


Figure 28 - CTS9513 Counter Mode X Representative Waveforms

MODE X HARDWARE SAVE

Mode X is a hardware edge triggered strobe counter with the capability of reading the counter value without interrupting the count.

As shown in Figure 28, once the counter is ARMed a valid gate edge starts the counter. Once triggered the counter will count to TC regardless of the state of the Gate line. Gate edges received prior to TC will store the current count in the Hold register. Once the counter has reached TC the counter will stop until a subsequent gate edge is received. Gate edges applied to an unarmed counter have no effect.

Symbol	Specification	Min	Max	Units
V_{ILT}	TTL Input LOW Level		0.8	Volts
V_{IHT}	TTL Input HIGH Level	2		Volts
V_{ILC}	X2 Input LOW Level		1.5	Volts
V_{IHC}	X2 Input HIGH Level	V_{DD} –1.5		Volts
V_{OL}	Output LOW Level @ I_{OL} = 4mA		0.4	Volts
V_{OH}	Output HIGH Level @ I_{OL} =4mA	2.4		Volts
I_Z	Input Leakage Current	-10	10	µA
I_{DD}	Supply Current /No Load / F_{OSC} = 7MHz		20	mA
I_{DDS}	IDD Static		10	µA
C_{IN}	Pin Capacitance		10	pF

Table 12 - CTS9513 Electrical Characteristics

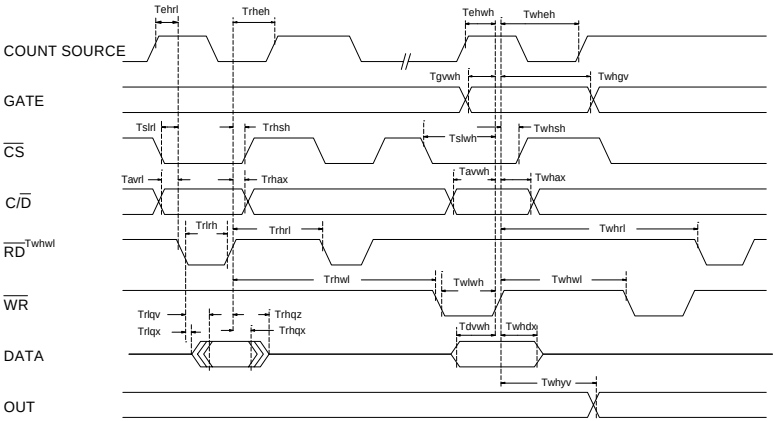


Figure 30 - Bus Timing Diagram

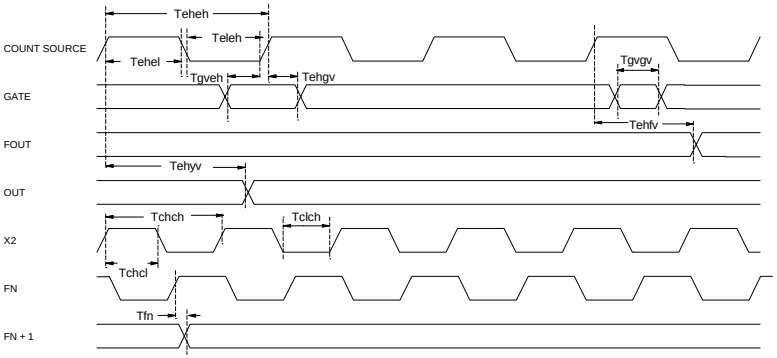


Figure 31 - Counter Timing Diagram

Param	Description	Figure	Min	Typ	Max	Units
Tavrl	C/D Valid to Read Low	2	0			nS
Tawwh	C/D Valid to Write High	2	0			nS
Tdvwh	Data In Valid to Write High	2	5			nS
Tehrl	Count Source High to Read (setup time) Note 2,7	2	10			nS
Tehwh	Count Source High to Write High (setup time) Note 3,7	2	10			nS
Tgvwh	Gate valid to Write High Note 3,10	2	10			nS
Trhax	Read High to C/D don't Care	2	0			nS
Trheh	Read High to Count Source High Note 4,7	2	0			nS
Trhqx	Read High to Data Out Invalid	2	3			nS
Trhqz	Read High to Data Out Hi-Z (Bus Release Time)	2			12	nS
Trhrl	Read High to Read Low (Read Recovery Time)	2	12			nS
Trhsh	Read High to CS High Note 12	2	2			nS
Trhwl	Read High to Write Low (Read Recovery Time)	2	16			nS
Trlqv	Read Low to Data Out Valid	2			15	nS
Trlqx	Read Low to Data Bus Driven (Bus Drive Time)	2			13	nS
Trlrh	Read Low to Read High (Read Pulse Duration) Note 12	2	12			nS
Tslrl	CS Low to Read Low Note 12	2	0			nS
Tslwh	CS Low to Write High Note 12	2	3			nS
Twhax	Write High to C/D Don't Care	2			16	nS
Twhdx	Write High to Data In Don't Care	2	2			nS
Twheh	Write High to Count Source High Note 5, 7, 14, 15	2	20			nS
Twhgv	Write High to Gate valid Note 5, 10, 14	2	20			nS
Twhrl	Write High to Read Low (Write Recovery Time) Note 16	2	16			nS
Twhsh	Write High to CS High Note 12	2	2			nS
Twhwl	Write High to Write Low (Write Recovery Time) Note 16	2	16			nS

Table 14 - Bus Timing Specifications

NOTES

1.
2. Any Input transition that occurs before this minimum setup requirement will be reflected in the contents read from the status register
3. Any Input transition that occurs before this minimum setup requirement will act on the counter before the execution of the operation initiated by the write and the counter may be off by one count
4. Any input transition that occurs after this minimum hold time is guaranteed to not influence the contents read from the status register on the current read operation
5. Any input transition that occurs after this minimum hold time is guaranteed to be seen by the counter as occurring after the action initiated by the write operation and the counter may be off by one count.
6. This parameter applies to cases where the write operation causes a change in the output bit.
7. The enabled count source is one of F1-F5, TCN-1 SRC1-SRC5 or GATE1-GATE 5, as selected in the applicable Counter Mode register. The timing diagram assumes the counter counts on rising source edges. The timing specifications are the same for falling-edge counting.
8. This parameter applies to edge gating (CM15-CM13=110 or 111) and gating when both CM7=1 and CM15-CM13?000. This parameter represents the minimum GATE pulse width needed to ensure that the pulse initiates counting or counter reloading.
9. This parameter applies to both edge and level gating (CM15-CM13=001 through 111 and CM7 =0). This parameter represents the minimum setup or hold times to ensure that the Gate input is seen at the intended level on the active source edge and the counter may be off by one count.
10. This parameter assumes that the GATENA input is unused (16-bit bus mode) or is tied high. In cases where the GATENA input is used, this timing specification must be met by both the GATE and GATENA inputs.
11. Signals F1-F5 cannot be directly monitored by the user. The phase difference between these signals will manifest itself by causing counters using two different F signals to count at different times on nominally simultaneous transitions in the F signals. F1=X2.
12. This timing specification assumes that CS is active whenever RD or WR are active. CS may be held active indefinitely.
13. This parameter assumes X2 is driven from an external gate with a square wave.
14. This parameter assumes that the write operation is to the command register.
15. This timing specification applies to single-action commands only (e.g. LOAD, ARM, SAVE, etc.) For double action commands such as LOAD AND ARM and DISARM AND SAVE, TWHEH minimum = 700ns.
16. In short data write mode, TWHRL and TWHWL minimum = 1000 ns.
17. This parameter applies to the hardware retrigger/save modes N, O, Q, R, and X (CM7 = 1 and CM15-CM13<>000). This parameter ensures that the gating pulse initiates a hardware retrigger/save operation.
18. This parameter applies to hardware load source select modes S and V (CM7 = 1 and CM15-CM13=000). This parameter represents the minimum hold time to ensure that the GATE input selects the correct load source on the active source edge.

Param	Description	Fig	Min	Typ	Max
Tchch	X2 Period	1		20	
Tchcl	X2 High Pulse Width	1		8	
Tclch	X2 Low Pulse Width	1		8	
Teheh	Count Source High to Count Source High (max count freq)	1		20	
Tehel	Count Source Pulse Duration - High	1		8	
Tehfv	Count Source high to FOUT Valid	1			64
Tehgv	Level Gating Hold Time (Note 1)	1		2	
Tehyv	Count Source High to Out Valid	1			32
Teleh	Count Source Pulse Duration - Low	1		8	
Tfn	Prescaler Clock Skew	1			10
Tgveh	Level Gating Setup Time (Note 1)	1		14	
Tgvgv	Gate Pulse Duration (Note 2)	1		5	

Table 15 - Counter Timing Specifications - To Accompany Figure 31

Notes
1 This parameter applies to both level and edge gating , representing the minimum setup or hold times to ensure that the Gate input is seen at the intended level on the active source edge or the counter may be off one count.
2 This parameter applies to both level and edge gating, representing the minimum gate pulse width needed to ensure the pulse initiates counter gating or reloading.